Errata

Title & Document Type: 5371A Frequency & Time Interval Analyzer Service Manual, Volume 2

Manual Part Number: 05371-90034

Revision Date: April 1, 1990

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

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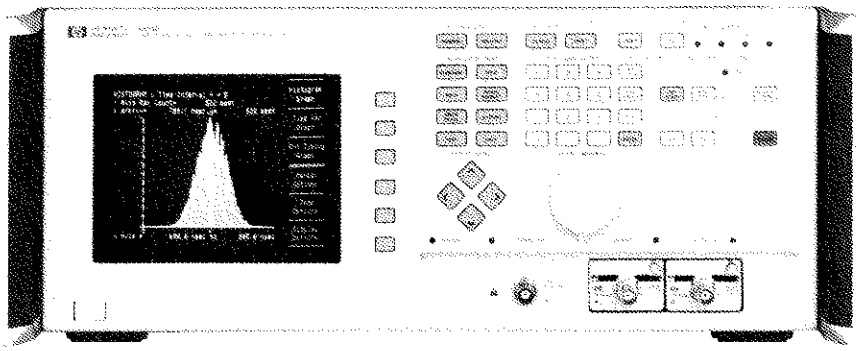
Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

HEWLETT-PACKARD

Service Manual
Volume 2

HP 5371A
Frequency and Time Interval Analyzer



1990

SERVICE MANUAL

Volume 2

HP 5371A
Frequency and Time Interval Analyzer

MANUAL APPLICABILITY

This manual applies directly to an HP 5371A having the serial number prefix listed below. If this number does not match your instrument, refer to the "Manual Updating Changes" included with this manual.

For additional important information about serial numbers, see INSTRUMENTS COVERED BY THIS MANUAL in the Introduction.

SERIAL NUMBER

Serial Number Prefix: 3018A

Edition 3
E0490

Manual Part Number 05371-90034
Microfiche Part Number 05371-90035

Printed APRIL 1990

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

This product is a Safety Class I instrument (provided with a protective earth terminal).

BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage and the correct fuse is installed. Refer to Operating Manual, Appendix B, INSTALLATION.

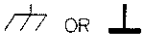
SAFETY EARTH GROUND

An uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

SAFETY SYMBOLS

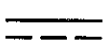
Instruction manual symbol; the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.



Indicates terminal is connected to chassis when such connection is not apparent.

Alternating current.



Direct current.

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a **CAUTION** sign until the indicated conditions are fully understood and met.

SAFETY INFORMATION

WARNING

Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two conductor outlet is not sufficient protection.)

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earthed pole terminal (neutral) of the power source.

Instructions for adjustments while covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform such adjustments or servicing unless qualified to do so.

For continued protection against fire, replace the line fuse(s) only with 250V fuse(s) of the same current rating and type (for example, normal blow, time delay). Do not use repaired fuses or short circuited fuseholders.

When measuring power line signals, be extremely careful and always use a step-down isolation transformer whose output voltage is compatible with the input measurement capabilities of this product. This product's front and rear panels are typically at earth ground, so **NEVER TRY TO MEASURE AC POWER LINE SIGNALS WITHOUT AN ISOLATION TRANSFORMER.**

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SECTION 7
SERVICE – GENERAL

7-1. INTRODUCTION

This section contains the information needed to service the HP 5371A. Service information includes diagnostics, component-level theory of operation, board block diagrams, troubleshooting procedures, test waveforms, component locators, schematic diagrams, cabling and assembly locations, disassembly and reassembly procedures, and signal descriptions and destinations. This information is organized as follows:

SECTION 7. SERVICE – GENERAL:

1. Safety Considerations – Describes the safety considerations applicable during maintenance, adjustments, and repair of the HP 5371A.

2. Troubleshooting – Provides a summary of troubleshooting procedures to isolate a fault to the functional or board level. Also included is the "Dead-Unit" troubleshooting procedure.

3. Electrostatic Discharge: Describes the precautions that must be taken to prevent damage to instrument assemblies and components.

4. Cleaning Printed Circuit Boards: Describes the cleaning of printed circuit boards following the soldering process.

5. Recommended Test Equipment: Refers to test equipment specified in *Table 1-2*.

6. Schematic Diagram Symbols and Reference Designations: Describes the symbols used on the schematic diagrams and the reference designators used for parts, subassemblies, and assemblies.

7. Identification Markings on Printed Circuit Boards: Describes the method used by Hewlett-Packard for identifying printed-circuit boards and assemblies, and lists all HP 5371A assemblies and their part numbers.

SECTION 7A. HP 5371A DIAGNOSTICS: Lists and describes the built-in diagnostics that can be used to verify various functional subsections of the counter's circuitry.

SECTION 7B. A1 TIMEBASE CONTROL/A14 TIMEBASE MULTIPLIER BOARDS: includes component-level theory of operation, troubleshooting procedures, block diagrams, component locators, and schematic diagrams for both the A1 and A14 assemblies.

SECTION 7C. A2 INPUT AMPLIFIER BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A2 assembly.

SECTION 7D. A4 INTERPOLATOR BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A4 assembly.

SECTION 7E. A5 ZDT/COUNT BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A5 assembly.

SECTION 7F. A6 DMA/GATE BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A6 assembly.

SECTION 7G. A7 PROCESSOR BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A7 assembly.

SECTION 7H. A8 I/O CONTROLLER BOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A8 assembly.

SECTION 7I. A9 DOUBLE REGULATOR BOARD: includes component-level theory of operation, component locator, and schematic diagram for the A9 assembly. The A9 Double Regulator Board is NOT field repairable. A10 TRIPLE REGULATOR BOARD: includes component-level theory of operation, component locator, and schematic diagram for the A10 assembly. The A10 Triple Regulator Board is NOT field repairable.

SECTION 7J. A11 FRONT PANEL BOARD: includes brief description, troubleshooting, component location, schematic diagram for the A11 assembly.

SECTION 7K. A12 MOTHERBOARD: includes component-level theory of operation, troubleshooting procedure, block diagram, component locator, and schematic diagrams for the A12 assembly.

SECTION 7L. A13 REAR PANEL BOARD: includes brief description, component locator, and schematic diagram for the A13 assembly.

SECTION 7M. DELETED. This section was originally intended for the A15 Oven Oscillator Assembly. This information is available in a separate manual for the HP 10811A/B Quartz Crystal Oscillator. See Manual Part Number 10811-90002.

SECTION 7N. ASSEMBLY AND CABLE LOCATIONS : lists the assembly reference designator, name, and HP Part Numbers of all HP 5371A assemblies. Also contains a list of the reference designation, HP Part Number, description, and destinations of all cabling used in the HP 5371A.

SECTION 7O. DISASSEMBLY AND REASSEMBLY: Describes procedures for removal of covers and assemblies to gain access to parts.

SECTION 7P. SIGNALS: lists signal name, logic level, source, destination, and function of all signals that connect daughter boards via the A12 Motherboard.

7-2. HP 5371A SERVICE KIT

HP has prepared a Service Kit which contains video service tapes, extender boards, extender cables, special cables, connectors, and technical manuals to service the HP 5371A. The video service tapes are supplied in both USA and PAL versions. The technical manuals include the Operating Manual, Programming Manual, and the two volumes of this Service Manual. An instruction sheet is included with the Service Kit describing the use of each item in the kit. The Service Kit Part Number is 05371-67001.

7-3. SAFETY CONSIDERATIONS

The HP 5371A is a Safety Class I instrument (provided with a protective earth terminal). Safety information pertinent to the maintenance of this instrument is included in this section.

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and to maintain the instrument in safe condition. Service instructions and adjustment procedures, which require the removal the top or bottom instrument covers, are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform any servicing or make any adjustments with the covers removed unless you are qualified to do so.

WARNING

THIS IS A SAFETY CLASS I PROVIDED WITH A PROTECTIVE EARTH TERMINAL. AN UNINTERRUPTABLE SAFETY EARTH GROUND MUST BE PROVIDED FROM THE MAINS POWER SOURCE TO THE HP 5371A INPUT WIRING TERMINALS, POWER CORD, OR SUPPLIED POWER CORD SET. WHENEVER IT IS LIKELY THAT THE PROTECTION HAS BEEN IMPAIRED, ANY INTERRUPTION OF THE PROTECTIVE GROUNDING CONDUCTOR INSIDE OR OUTSIDE THE INSTRUMENT OR OPENING THE PROTECTIVE EARTH TERMINAL WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY. INTENTIONAL INTERRUPTION IS PROHIBITED. THE INSTRUMENT MUST BE MADE INOPERATIVE AND BE SECURED AGAINST ANY UNINTENDED OPERATION.

IF THE HP 5371A IS TO BE ENERGIZED VIA AN EXTERNAL AUTOTRANSFORMER FOR VOLTAGE REDUCTION, MAKE SURE THAT THE COMMON TERMINAL IS CONNECTED TO THE EARTH POLE OF THE POWER SOURCE. FAILURE TO GROUND THE INSTRUMENT CAN RESULT IN PERSONAL INJURY. REFER TO THE PARAGRAPH TITLED "Power Cable".

WARNING

THE AC POWER CIRCUITS TO TRANSFORMER T1, FAN B1, AND THE A12 MOTHERBOARD ARE ALWAYS ENERGIZED WHEN THE INSTRUMENT IS CONNECTED TO AC MAINS REGARDLESS OF THE SETTING OF THE FRONT-PANEL POWER SWITCH (STBY-ON). THE +25 VDC (UNREGULATED) ON THE A12 MOTHERBOARD, THE UNREGULATED DC VOLTAGE TO THE A7 PROCESSOR BOARD (BACK-UP RAMS U50 AND U51, REAL-TIME CLOCK U46), AND THE REGULATED DC VOLTAGE TO THE A15 OVEN OSCILLATOR HEATER ARE ALSO ALWAYS ON WHEN THE AC POWER IS CONNECTED TO THE HP 5371A, EVEN WHEN THE FRONT-PANEL STBY-ON SWITCH IS SET TO STBY. CONTACT WITH ANY OF THESE CIRCUITS CAN RESULT IN PERSONAL INJURY OR DAMAGE TO EQUIPMENT.

WARNING

WHEN THIS INSTRUMENT IS CONNECTED TO THE POWER MAINS, DANGEROUS VOLTAGES ARE ALWAYS LOCATED INSIDE THE INSTRUMENT, REGARDLESS OF THE POSITION OF THE STBY-ON (POWER) SWITCH.

WARNING

TO PREVENT CATHODE-RAY TUBE (CRT) IMPLOSION, AVOID HANDLING OR JARRING OF THE CRT DISPLAY UNIT. BREAKAGE OF THE CRT CAUSES A HIGH-VELOCITY SCATTERING OF GLASS FRAGMENTS (IMPLOSION). HANDLING THE CRT MUST BE DONE ONLY BY QUALIFIED MAINTENANCE PERSONNEL USING APPROVED SAFETY MASK AND GLOVES.

WARNING

ANY ADJUSTMENT, MAINTENANCE, AND REPAIR OF THE OPENED, ENERGIZED INSTRUMENT SHOULD BE AVOIDED WHEN POSSIBLE. BUT, IF NECESSARY, SUCH TESTING SHOULD BE PERFORMED BY A SKILLED PERSON WHO IS AWARE OF THE HAZARDS INVOLVED. CAPACITORS INSIDE THE INSTRUMENT, SUCH AS C1, MAY STILL BE CHARGED EVEN IF THE INSTRUMENT HAS BEEN DISCONNECTED FROM ITS AC POWER SOURCE.

WARNING

IF, DURING MAINTENANCE, IT BECOMES NECESSARY TO REMOVE THE SAFETY SHIELD INSULATORS (MP37) THAT COVER THE MOTHERBOARD HIGH VOLTAGE AREA OR THE LOW VOLTAGE (BUT POTENTIALLY HIGH CURRENT) BRIDGE DIODE CR1, ENSURE THAT THEY ARE REPLACED WHEN WORK IS COMPLETED.

WARNING

REMOVE ALL JEWELRY (RINGS, BRACELETS, ETC.) WHEN WORKING WITHIN THE HP 5371A. HIGH VOLTAGES ARE PRESENT WITHIN THE POWER SUPPLY SAFETY COVER WHILE A LOW VOLTAGE-HIGH CURRENT HAZARD EXISTS NEAR BRIDGE RECTIFIER CR1.

WARNING

THE HP 5371A WEIGHS 23.2 KG (51 LBS). CARE MUST BE TAKEN WHEN LIFTING THE INSTRUMENT TO AVOID PERSONAL INJURY. USE EQUIPMENT SLIDES WHEN RACK MOUNTING. (REFER TO "OPTIONS" PARAGRAPHS IN SECTION 1 FOR DETAILS.)

CAUTION

BEFORE PLUGGING THE HP 5371A into the Mains (line) voltage, be sure the correct line voltage and fuse have been selected. You must set the voltage selector turret wheel correctly to adapt the HP 5371A to the power source available. Refer to the paragraph titled "Line Voltage and Fuse Selection".

CAUTION

The HP 5371A top and bottom covers are unique to the HP 5371A and therefore must remain with the instrument at all times. Both covers are insulated so replacing either one with the covers from another instrument could result in damage to the HP 5371A.

CAUTION

Make sure that only fuses with the required current and voltage ratings, and of the specified type (normal blow, time delay, etc.), are used for replacement. DO NOT USE shorted circuit fuseholders or repaired fuses.

7-4. Safety Symbols

The safety symbols used on equipment and in manuals are shown in *Table 7-1.*

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

This product is a Safety Class I instrument (provided with a protective earth terminal).

BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage and the correct fuse is installed. Refer to Operating Manual, Appendix B, INSTALLATION.

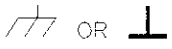
SAFETY EARTH GROUND

An uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

SAFETY SYMBOLS

Instruction manual symbol; the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.



Indicates terminal is connected to chassis when such connection is not apparent.

Alternating current.

Direct current.

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a **CAUTION** sign until the indicated conditions are fully understood and met.

SAFETY INFORMATION

WARNING

Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two conductor outlet is not sufficient protection.)

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earthed pole terminal (neutral) of the power source.

Instructions for adjustments while covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform such adjustments or servicing unless qualified to do so.

For continued protection against fire, replace the line fuse(s) only with 250V fuse(s) of the same current rating and type (for example, normal blow, time delay). Do not use repaired fuses or short circuited fuseholders.

When measuring power line signals, be extremely careful and always use a step-down isolation transformer whose output voltage is compatible with the input measurement capabilities of this product. This product's front and rear panels are typically at earth ground, so **NEVER TRY TO MEASURE AC POWER LINE SIGNALS WITHOUT AN ISOLATION TRANSFORMER.**

7-5. After Service Product Safety Checks

The following safety checks must be performed after any troubleshooting and repair procedures have been completed to ensure the safe operation of the instrument.

WARNING

RESISTANCE CHECKS DESCRIBED BELOW REQUIRE THAT THE POWER CORD BE CONNECTED TO THE THE HP 5371A AND THAT AC POWER BE DISCONNECTED. BE SURE THAT THE POWER CORD IS NOT CONNECTED TO POWER BEFORE PERFORMING ANY SAFETY CHECKS.

A. VISUAL INSPECTION. Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

B. GROUND CONTINUITY TEST. Plug the power cord (W22) into the rear-panel power module. (DO NOT CONNECT THE INSTRUMENT TO AC POWER.) Using a suitable ohmmeter, check resistance from the instrument enclosure (chassis) to the ground pin on the power cord plug. The reading must be less than 1Ω. Flex the power cord while making this measurement to determine whether intermittent discontinuities exist.

C. Check any indicated front- or rear-panel ground terminals marked, using the above procedure.

D. INSULATION RESISTANCE TEST. Tie the line and neutral pins of the power cord plug together. Measure the resistance from the instrument enclosure (chassis) to the line and neutral pins of the power cord plug. The minimum acceptable resistance is 2 MΩ. Replace any component which results in a failure.

E. A16 POWER MODULE CHECK. Check the line fuse and the power line selector (turret wheel) to verify that the correctly rated fuse is installed and that the instrument is properly set for the AC power source applied.

7-6. TROUBLESHOOTING

7-7. Introduction

The following paragraphs describe procedures for troubleshooting the HP 5371A. The techniques described are designed to isolate a fault to the component level. The following summary of the troubleshooting procedures provides a guide to assist you in selecting the appropriate procedure to use when a particular HP 5371A failure occurs.

SUMMARY OF HP 5371A TROUBLESHOOTING PROCEDURES

FAILURE SYMPTOMS	TROUBLESHOOTING PROCEDURE
1. Dead Instrument – No Display	Dead Instrument
2. Diagnostic Test 2 Time Base Failed	A1 & A14 Timebase Control and Multiplier Assemblies
3. Diagnostic Test 3 Input Pods	A1 & A14 Timebase Control and Multiplier Assemblies
4. Error 107 500 MHz Oscillator Out of Lock	A1 & A14 Timebase Control and Multiplier Assemblies
5. Measurement Accuracy is 2 ns or worse	A4 Interpolator Assembly
6. Unstable Measurements	A4 Interpolator Assembly
7. Diagnostic Test 5 Count ICs: ZDT3A and ZDT3B Failed	A4 Interpolator Assembly
8. Diagnostic Test 5 Count ICs Failed	A5 ZDT/Count Assembly
9. Diagnostic Test 7 Measurement RAM Failed	A5 ZDT/Count Assembly
10. Large miscount errors	A5 ZDT/Count Assembly
11. Front Panel Lock Up	A6 DMA/Gate Assembly
12. Diagnostic Test 5 Count ICs and Diagnostic Test 7 Measurement RAMs both have all failed.	A6 DMA/Gate Assembly
13. Diagnostic 7 Measurement RAMs have all failed and/or all Interpolator RAMs have all failed.	A6 DMA/Gate Assembly
14. HP-IB Dump Mode failing	A6 DMA/Gate Assembly
15. HP 5371A display never gets updated.	A6 DMA/Gate Assembly
16. Diagnostic Test 7 Measurement RAMs indicate failure with Interpolator RAMs.	A6 DMA/Gate Assembly
17. Incorrect Measurement Results	A6 DMA/Gate Assembly
18. Diagnostic Test 6 Gate Timer Fails	A6 DMA/Gate Assembly
19. HP 5371A External Arm Input not functioning.	A6 DMA/Gate Assembly
20. HP 5371A Totalize function not working.	A6 DMA/Gate Assembly
21. Diagnostic Test 8 System ROM Failed	A7 Processor Assembly

22. Diagnostic Test 9 System RAM Failed	A7 Processor Assembly
23. Diagnostic Test 10 Timer Failed	A7 Processor Assembly
24. Diagnostic Test 11 Real Time Clock Failed	A7 Processor Assembly
25. Diagnostic Test 12 CRT RAM Failed	A8 I/O Control Assembly
26. Diagnostic Test 13 LED Latch Failed	A8 I/O Control Assembly
27. Diagnostic Test 14 CRT Controller Failed	A8 I/O Control Assembly
28. Diagnostic Test 15 Key Controller Failed	A8 I/O Control Assembly
29. Diagnostic Test 16 DMA Controller Failed	A8 I/O Control Assembly

7-8. Dead-unit Troubleshooting

This section is to be followed when the screen diagnostics are unusable.

NOTE

EXTREMELY HIGH VOLTAGE LEVELS ARE PRESENT IN THE AREA OF THE CATHODE RAY TUBE (CRT) AND DRIVER BOARD ASSEMBLY WHEN THE HP 5371A IS CONNECTED TO AC POWER. USE EXTREME CAUTION WHEN TROUBLESHOOTING WITH THE POWER SUPPLY COVER REMOVED.

A. Check line fuse and line voltage setting.

B. Measure voltage regulators as shown in *Figure 7-1*.

1. The regulators are interlocked as follows:

   - The A10 Triple Regulator (+5v, +15V, and –15V) SHUTDOWN input must be at a low (0V.) logic level. (This level will be measured in Step C.)
   - The –15V must be present before the the +5V and +15V can come up.
   - The A9 Dual Regulator (–5.2V and –3.3V) will not come up until the A10 Triple Regulator is operating.

2. If either of the regulators are faulty, replace with new cards.

C. Measure voltages and signals on the bottom side of the A12 Motherboard as shown in *Figure 7-2*.

D. If the CRT screen is blank and the input signals +12, VIDEO, HSYNC, and VSYNC are present on the A12 Motherboard, replace the CRT assembly. The CRT is replaceable as a complete unit (CRT and Driver Board). You may want to swap just the PC board portion first to see if that fixes the problem.

E. If the A9 and A10 Regulator, and A12 Motherboard voltages are okay, continue troubleshooting the A7 Processor and A8 I/O Controller boards.

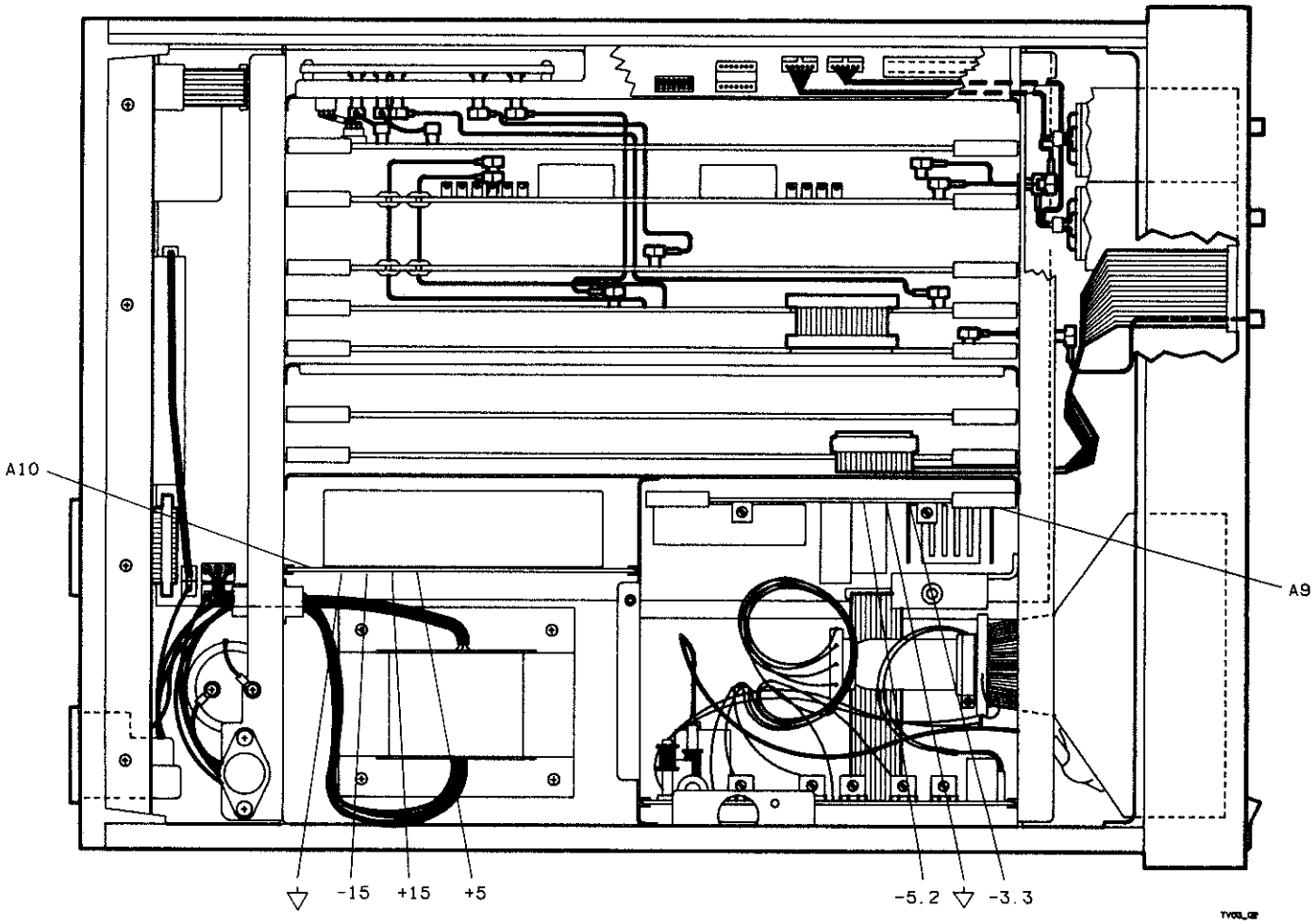


Figure 7-1. HP 5371A Power Supply Locator (Instrument Top View)

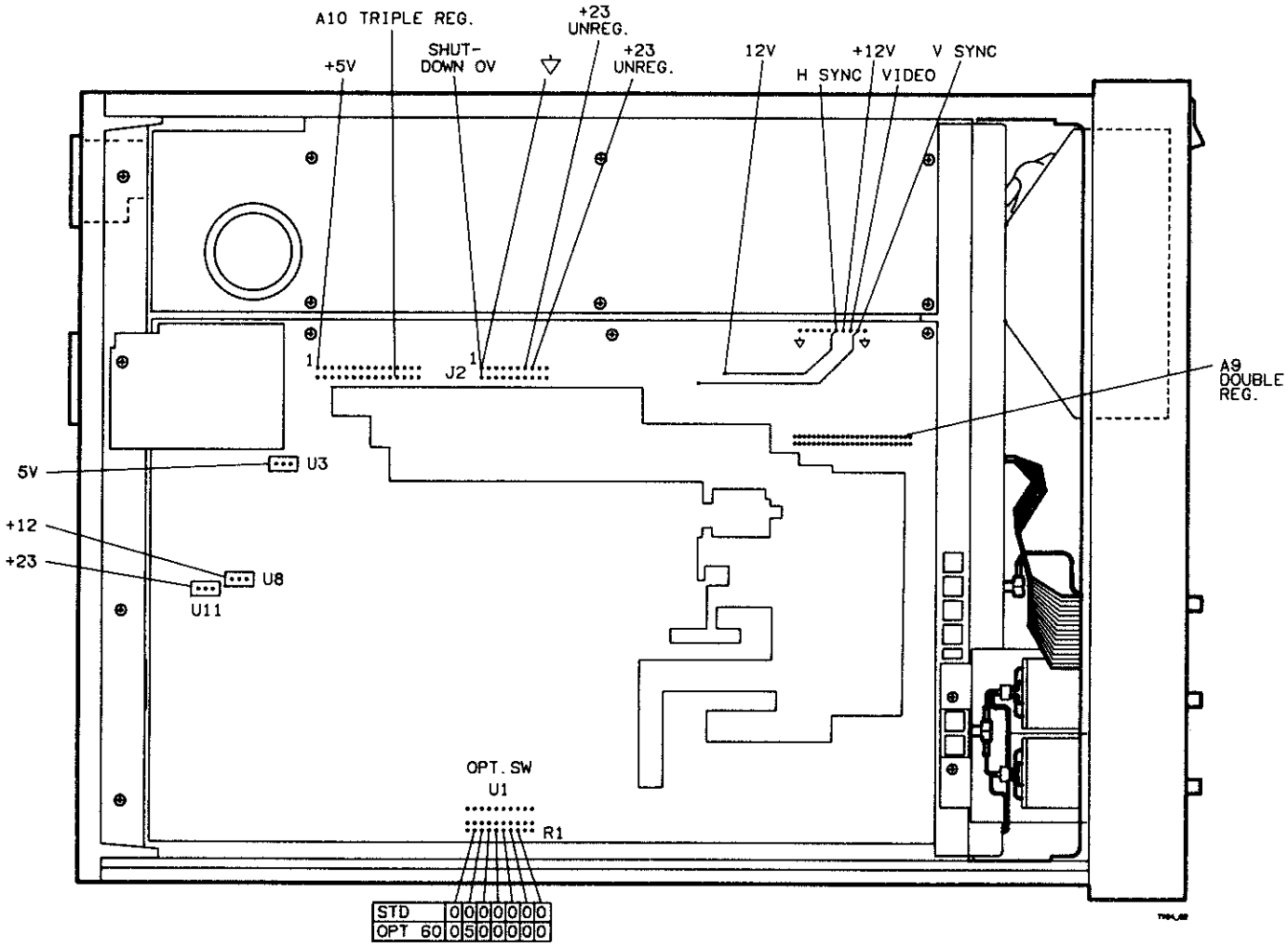


Figure 7-2. Motherboaard Voltage Probe Locator

7-9. ELECTROSTATIC DISCHARGE

Electronic components and assemblies in the HP 5371A can be permanently degraded or damaged by electrostatic discharge. Use the following precautions when servicing the instrument:

A. ENSURE that the static sensitive devices or assemblies are serviced at static safe work stations providing proper grounding for service personnel.

B. ENSURE that static-sensitive devices or assemblies are stored in static shielding bags or containers.

C. DO NOT wear clothing subject to static buildup, such as wool or synthetic materials.

D. DO NOT handle components or assemblies in carpeted areas.

E. DO NOT remove an assembly or component from its static shielding protection until you are ready to install it.

F. AVOID touching component leads. (Handle by the packaging only.)

7-10. CLEANING PRINTED-CIRCUIT BOARDS

After soldering a component to a printed-circuit (PC) board, HP recommends that you DO NOT remove the flux from the soldered area. It has been found that after a hand soldering operation, the solder flux from RMA-P2 (Rosin, Mildly Active) solder does no harm if left in place on a PC board; the flux residue is inert and non-conductive. However, when the flux is dissolved with a chemical, in an attempt to remove it from the board, it spreads over the board, releasing several activators (chlorides, bromides, etc.). Now, instead of having a harmless flux residue with the water soluble activators trapped inside, you have a potential corrosion problem. If the instrument is stored in a humid environment, over time moisture will be absorbed which can start the corrosion process.

7-11. RECOMMENDED TEST EQUIPMENT

Test equipment recommended for testing (performance tests and/or adjustments) and troubleshooting the HP 5371A is listed in *Table 1-2*. Substitute equipment may be used if it meets or exceeds the required characteristics listed in the table.

7-12. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATIONS

Figure 7-3 shows the various common symbols used on the schematic diagrams. At the bottom of *Figure 7-3*, the identification system for reference designators, assemblies, and subassemblies is shown.

7-13. Reference Designators

Reference designators are assigned to indicate the class and the location of printed circuit assemblies (boards), subassemblies (if any), and all of the component parts, as shown in the example in *Figure 7-3*. Assemblies are assigned numbers in sequence — A1, A2, etc. Component parts are numbered in sequence, from left to right, top to bottom, according to the physical location on the assembly.

Subassemblies within an assembly are given a subordinate "A" number. For example, the rectifier subassembly A1 of *Figure 7-3* has a complete designation of A25A1. For individual components, the complete designation is determined by adding the assembly number and subassembly number, if any. For example, CR1 would have a complete reference designator of A25A1CR1.

7-14. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

Printed-circuit boards in the HP 5371A have four identification numbers: an assembly part number, a serial number, a revision letter, and a production code.

The assembly part number has 10 digits, as in 05371-60011, and is the primary identification. All assemblies with the same part number are interchangeable. When a production is made on an assembly that renders it incompatible with previous assemblies, the part number is changed.

The serial number consists of a five digit prefix and a five digit unique serial number i.e., PPPPP-SSSSS. The prefix is used to determine if engineering changes have been made to the board. The manual change sheet or the backdating section of this manual documents the range of prefix numbers that apply to a particular board configuration.

Revision letters, A, B, etc., denote changes in printed circuit layout. For example, if a capacitor type is changed, physically as opposed to electrically, and requires different spacing for its leads, the printed-circuit layout is changed and the revision number is incremented to the next letter.

The production code is a four-digit, seven segment number used for production purposes.

SYMBOLS

DANGEROUS VOLTAGE, EXCEEDS 1000 VOLTS

FRONT PANEL LABEL

REAR PANEL LABEL

INTERIOR AND PC BOARDS LABEL

WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE

OR PROTECTIVE CONDUCTOR TERMINAL

CIRCUIT COMMON

IDENTIFIED COMMON

OR CHASSIS TERMINAL

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

OR OR TEST POINT

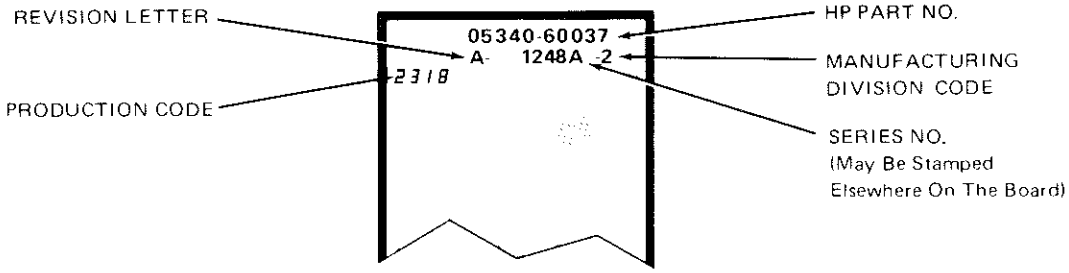
INSTRUCTION MANUAL REFERENCE

ALTERNATING CURRENT

DIRECT CURRENT

ALTERNATING OR DIRECT CURRENT

PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

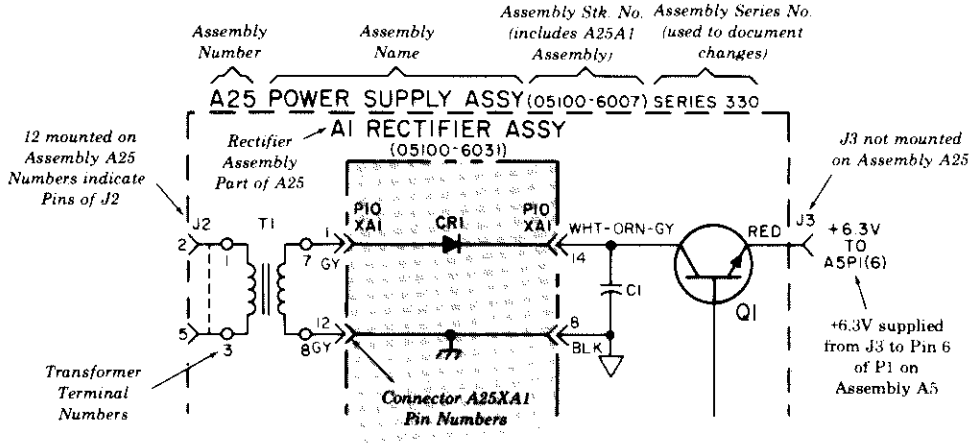


Figure 7-3. Schematic Diagram Notes

7-15. IDENTIFICATION AND REPAIR OF MULTILAYER CIRCUIT BOARDS

Multi-layer circuit boards with conductors in three or more layers have a rectangular pattern of 4, 6, or 8 windows with single digits visible in the windows when viewed over a light. The square windows appear on both sides of the circuit board. The number of identifiable numbers indicate the number of layers in the circuit board. For, example, a circuit board having four windows with a "1" in one window, a "4" in a second window (on the opposite side of the board), a "2" or "3" visible through the third window, and one window that's blank, the board has three layers.

CAUTION

Multi-layer circuit boards are susceptible to damage from heat or excessive force applied when removing or replacing parts. Static-free vacuum devices that pull the molten solder out of the circuit board's feedthrough holes are required. With the solder effectively removed, parts should be easy to remove with excessive prying or pulling on component leads.

7-16. LOGIC SYMBOLS

Logic symbols used in this manual conform to the American National Standard publication *EEE Standard Graphic Symbols for Logic Functions, ANSI/IEEE Std. 91-1984*. This standard supercedes MIL-STD-806B. Another useful reference source is *The TTL Data Book*, "Explanation of New Logic Symbols" by F.A. Mann (Texas Instruments Incorporated).

7-17. ROUTINE MAINTENANCE

The only routine maintenance required is the periodic cleaning of the front-panel CRT protective anti-glare filter screen. The filter may be cleaned as follows:

A. WHILE THE FILTER IS INSTALLED IN THE INSTRUMENT.

1. Method 1. Wipe the mesh with a lint-free cloth that has been dampened with isopropyl alcohol.

2. Method 2. Use compressed air to blow off any dirt particles on the filter.

NOTE

DO NOT USE any type of cloth or tissue paper which may contaminate the filter with particles.

B. WHEN THE FILTER IS REMOVED FROM THE INSTRUMENT. Clean the filter with a lint-free cloth that has been dampened with warm, soapy water. Use a light, rubbing motion to clean the filter mesh. Rinse the filter thoroughly by holding it under warm, running water. Dry the filter using two lint-free cloths, rubbing the mesh from both sides simultaneously.

Refer to the filter removal procedure described in the disassembly instructions in this manual section if filter cleaning or replacement is required.

7-18. OPERATING ENVIRONMENT

7-19. Temperature

The instrument may be operated in temperatures that range between 0 and 40°C.

7-20. Humidity

The HP 5371A may be operated in environments with humidity from 5% to 95% at temperatures that range between 0 and 40°C.

7-21. Altitude

The HP 5371A may be operated at altitudes up to 4,572 metres (15,000 feet).

7-22. POWER REQUIREMENTS

The HP 5371A can operate from power sources of 100-, 120-, 220-, or 240-volt AC, ±10%, at 50 to 60 Hertz. Maximum power consumption is 500 volt-amperes. (See "SAFETY CONSIDERATIONS" for additional information.)

7-23. LINE VOLTAGE AND FUSE SELECTION

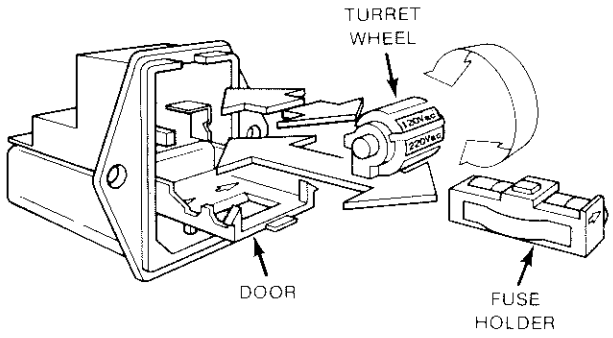
CAUTION

BEFORE PLUGGING THE HP 5371A into the Mains (line) voltage, be sure the correct line voltage and fuse have been selected. You must set the voltage selector turret wheel correctly to adapt the HP 5371A to the power source available. Refer to the paragraph titled "Line Voltage and Fuse Selection".

The HP 5371A is equipped with a power module (A16 Power Module Cable Assembly located on the instrument's rear panel) that contains a turret wheel line voltage selector that allows you to select either 100-, 120-, 220-, or 240-volt AC operation as shown in *Figure 7-4*. Before applying power to the HP 5371A, the turret wheel selector must be set to the correct position and the correct fuse must be installed as described in the following paragraph.

Power line connections are selected by the position of the plug-in turret wheel in the A16 module. The correct value fuse, with a 250-volt rating, must be installed before the turret wheel is inserted. The HP 5371A uses a 4 Ampere fuse (HP Part Number 2110-0055) for 100/120-volt operation and a 2 Ampere fuse (HP Part Number 2110-0002) for 220/240-volt operation.

To change the line fuse, disconnect power cord W22 from the A16 module and then follow the instructions in *Figure 7-4.*



SELECTION OF OPERATING VOLTAGE

1. Using a small, flat-head screwdriver, snap open the power module door to access the fuse and turret wheel.
2. REMOVE the turret wheel before turning to desired voltage. DO NOT turn turret wheel while installed in module. Push wheel firmly into module slot.
3. To change or install fuse, pull fuse holder and re-insert fuse in holder, using caution to select correct fuse value. Re-insert fuse and holder.
4. Close the power module door. The selected operating voltage is shown in module window.

Figure 7-4. Line Voltage Selection Using A16 Power Module Turret Wheel

In addition, the HP 5371A has two internal, low-voltage fuses;

a 10 Ampere fuse, A9F1, that protects the +25V Unregulated input to the A9 Double Regulator Board (HP P/N 2110-0713), and a thermal fuse, A15F1, contained within the A15 Oven Oscillator (HP P/N 2110-0617).

7-23. FRONT-PANEL LED ANNUNCIATORS

Several front-panel LED annunciators provide a visual indication of several of the instrument's status conditions. Two examples of status conditions are the HP-IB configuration and the trigger state.

7-24. HP-IB Status LEDs

RMT – The RMT annunciator LED is ON when HP 5371A is under remote control.

LSN – The LSN annunciator LED is ON when the HP 5371A is addressed to listen.

TLK – The TLK annunciator LED is ON when the HP 5371A is addressed to talk, or when it is being used in the TALK ONLY mode.

SRQ – The SRQ annunciator LED is ON when the HP 5371A sends a service request to the controller in charge of the HP-IB.

7-26. Instrument Control LEDs

GATE – The GATE annunciator LED shows the status of the HP 5371A's counter gate. Before a measurement starts, this LED is OFF, indicating the gate is closed. During a measurement, this LED turns ON, indicating the gate is open. When the gate duration is less than or equal to 100 milliseconds, the GATE LED remains ON for a minimum of approximately 100 milliseconds.

SINGLE – When the SINGLE annunciator LED is ON, the counter makes a single measurement and displays the result.

7-27. EXTERNAL ARM, CHANNEL A, and CHANNEL B LEDs

All three of these LEDs provide a visual indication of the triggering status of each respective channel. If one of the three LEDs is flashing at a 10-Hz rate, the respective channel is triggering. If one of the LEDs is OFF the input signal to the respective channel is either above or below the trigger level setting.

7-28. STANDBY LED and Power (STBY-ON) Switch

When the STBY-ON switch is in the ON position, power is supplied to the entire instrument. The STBY position removes normal operating power to the instrument, but continues to supply power to both the A15 Oven Oscillator's internal oven to maintain a constant temperature for its crystal, and to two backup RAM ICs (A7U50 and U51) located on the A7 Processor Board. The front-panel STANDBY annunciator LED is ON when the switch is set to STBY. This means that the input to the main chassis-mounted transformer T1, and consequently the unregulated +25 Volts DC to the A15 oscillator oven and the LP voltage to the A7 backup RAMs are always energized whenever AC power is connected, regardless of the STBY-ON switch setting.

Note that the HP 5371A's A7 Processor Board is equipped with an internal battery for continuous memory storage of up to 10 separate front panel settings. The battery is NOT rechargeable.

7-29. Keyboard Memory

Whenever the HP 5371A is set to Standby, the 68000 microprocessor automatically stores the front-panel settings in memory energized by a back-up battery power supply. This avoids having to re-enter math constants, functions or input setups, whenever the instrument is set to Standby, AC power is removed from the instrument, or the A7 Processor Board is physically removed from the instrument.

7-30. HEWLETT-PACKARD INTERFACE BUS (HP-IB)

7-31. HP-IB Connections

The HP 5371A communicates over the HP-IB via the 24-pin connector located on the instrument's rear panel. The connector is compatible with the HP 10833A/B/C/D HP-IB cables. The HP-IB system allows the user to connect up to 15 (including the system controller) HP-IB compatible instruments. The HP-IB cables have identical "piggy-back" connectors at both ends of the cable allowing several cables to be connected to a single source without the need of special adapters or switch boxes.

7-32. HP-IB Address Selection

The HP-IB device address of the HP 5371A is selected from its front panel via the SYSTEM Menu screen. The address applies to both talk and listen functions. The selectable addresses range from 0 to 30. Instructions the selecting the address can be found in Section 12 of the Operating Manual. The default address value is "3" and is retained in the non-volatile CMOS memory (A7U50 and U51) located on the A7 Processor Board.

7-33. HP-IB Descriptions

A description of the Hewlett-Packard Interface Bus (HP-IB) is provided in the HP 5371A Programmer's Manual.

7-34. LOGIC FAMILY VOLTAGE LEVELS

The HP 5371A uses four types of logic devices. They are:

A. Transistor-Transistor-Logic (TTL)

B. Emitter-Coupled Logic (ECL)

C. Emitter-Emitter-Coupled Logic (EECL)

D. Emitter-Function Logic (EFL)

Table 7-2. Logic Levels

Logic State	TTL	ECL	EECL	EFL
HIGH	+2.0V to +5.0V	–0.9V	0.0V	+2.1V
LOW	0V to +0.8V	–1.8V	–0.6V	+1.5V

7A DIAGNOSTICS

SECTION 7A
DIAGNOSTICS

7A-1. INTRODUCTION

The HP 5371A Frequency and Time Interval Analyzer is a 68000 μP-based system having built-in diagnostics. These diagnostics aid in testing and troubleshooting the instrument by identifying faulty assemblies (i.e., A1, A2, etc.). All diagnostics are accessible via the front-panel CRT Display and over the HP-IB. (Detailed HP-IB information can be found in the Programming Manual.) There are three types of diagnostics:

a. *Power-up Self Test:* A sequence of tests automatically executed when the instrument is powered up. When power is initially applied to the 5371A, the "PERFORMING SELF TEST..." message is displayed. After 10-15 seconds, and if all tests have passed, the "Frequency" FUNCTION screen is displayed.

b. *Self Test:* A sequence of tests executed by selecting "Self Test" accessible via the TEST menu displayed on front-panel CRT.

c. *User-callable Diagnostics:* Individual tests that exercise specific circuitry within the 5371A.

7A-2. HP-IB COMMANDS FOR CALLING DIAGNOSTIC TESTS

There are three HP-IB commands for implementing diagnostic testing: the TEST command and the TEST? and *TST? queries.

The TEST command executes the diagnostic test corresponding to the test number sent with the command. The test numbers are:

Test Number	Test Name	Test Number	Test Name
1	Self Test	12	CRT RAM
2	Timebase	13	LED Latch
3	Input Pods	14	CRT Controller
4	Input Amplifiers]	15	Key Controller
5	Count ICs	16	DMA Controller
6	Gate Timer	17	Front Panel
7	Measurement RAM	18	CRT Adjustment
8	System ROM	19	CRT Video Pattern
9	System RAM	20	External Amplifier
10	Timer	21	Calibrate Interpolators
11	Real-Time Clock		

The TEST? query returns the PASS/FAIL status and message of the last diagnostic test executed.

The *TST? query initiates a series of self tests that exercise various circuits of the 5371A, and is equivalent to the Self Test selection in the Diagnostic Test screen. All tests performed require no user interface and do not affect data stored in System and CRT Display RAM. Measurement data stored in Measurement RAM will be lost. The *TST query returns "PASS" when all tests pass, or returns the test number and associated message of the first test that fails.

7A-3. HELP MENU SCREENS

The 5371A provides a set of HELP menu screens that give the user brief description of all features accessible from the front panel. A simplified functional block diagram is also provided by the HELP menu. Selecting one of the options below, changes the softkey selections providing references to additional menus for each of the eight options listed below:

- FUNCTION Menu — Provides measurement setup information such as arming overview, valid arming options, measurement and block size.
- INPUT Menu — Provides description of Channel A and B, choices of determining input trigger voltage levels, input channel characterization, and Separate/Common input modes.
- MATH Menu — Provides description of math modifiers, statistics, limit testing, and set reference.
- RESULTS Menu — Provides description of CRT Display options for reviewing measurement results. ASCII, Floating Point, and Binary measurement result format choices are also described.
- USER INTERFACE Menu — Provides description of front-panel Menu keys associated with entry of numeric data, INSTRUMENT CONTROL keys, INSTRument STATE key, and more. Three types of error messages are also described.
- GRAPHS Menu — Provides description of histogram, time variation, and event timing graphs that can be generated by the 5371A. Softkey levels for access to graphics data are also described.
- HP-IB Menu — Provides description of HP-IB command format, HP-IB Status Byte, Event Status, and Hardware Status Registers.
- TEST Menu — Provides brief description of how to select and run all diagnostic tests.

7A-4. DIAGNOSTICS

When instructed to do so, the 5371A performs diagnostics that verify the overall operation of the instrument and identify any defective assemblies or component parts. These tests are accessed via the TEST menu from the front-panel CRT display, or over the HP-IB using the TEST command. A subset of the diagnostic tests are automatically executed during power-up initialization or system reset.

7A-5. Power-up Self Tests

The tests executed during power-up are those requiring no user interaction. If a failure is detected, an explanatory error message is displayed on the instrument's CRT. When all diagnostics are completed, the 5371A pauses and waits for the user to press any front-panel key. After the key has been pressed, the instrument attempts to operate in a normal fashion even though a failure has been detected. The following tests are executed during the power-up process:

- System RAM Test
- Back-up RAM Test
- CRT RAM Test
- Front Panel Controller Initialization Test

- System ROM Test
- Timer Test
- Real-time Clock Test
- CRTC Test
- DMA Test
- LED Latch Test
- Time Base Test
- Count ICs Test
- Measurement RAM Test
- Gate Timer Test
- Input Amplifier Test
- Input Pod Test

The System RAM, CRT Display RAM, and Measurement RAM tests, which are performed during power-up initialization, check for unique address locations and therefore are destructive to the data contained in the RAM locations. The only data retained during the RAM tests is that stored in the CMOS battery back-up ICs, A7U50 and U51. Less comprehensive and therefore non-destructive System and CRT RAM Display RAM tests are used after power-up to prevent loss of data during testing. Testing performed on the Measurement RAMs is always destructive to data.

The Back-up RAM and the Front Panel Controller Initialization Tests are performed only during the power-up testing sequence. A description of each test follows.

7A-6. BACK-UP RAM TEST

This test checks back-up RAMs A7U50 and A7U51 which are powered by battery A7BT1 during AC power loss. These RAMs contain variables that are saved when the instrument is powered down. When the 5371A is powered down, the 68000 μP performs a checksum test for back-up RAM memory space. When the instrument is powered up, the checksums are again calculated and should match those saved at power-down. If the checksums do not match, all the variables in the back-up RAM memory space are initialized to default values. This test is performed only during the power-up tests and is not accessible to the user.

Messages:

Back-up RAM PASSED
Instrument setup lost. Reset to default.

If the checksums for the System RAM space containing the instrument setup are not correct, this message is displayed at instrument power-up.

Saved configuration lost.

If the checksums for the System RAM space containing the saved instrument setups are not correct, this message is displayed at instrument power-up.

7A-7. FRONT PANEL KEYBOARD CONTROLLER INITIALIZATION TEST

Prior to writing a parameter to the Front Panel keyboard Controller IC, A8U1, the 68000 μP waits for the controller to set bit 1 of the key-status register to 0. If this does not occur before a software wait loop times out, this test will fail. This test is performed during power-up sequence only.

7A-8. TEST Menu Screen

All tests available to the user via the 5371A front panel are shown on the TEST Menu Screen. The following tests are available:

- Instrument Self Test
- Hardware/Memory Diagnostics
- Front Panel Hardkey, Softkey, ENTRY/MARKER RPG, and HP-IB STATUS/INSTRUMENT CONTROL LED Check
- CRT Adjustment Routine
- EXTERNAL ARM Amplifier Test
- Interpolator Calibration Routine

The TEST Menu Screen is accessed by pressing the front-panel TEST key. The test highlighted on the menu screen by the cursor is executed if the Run softkey is pressed. The cursor can be moved by pressing the arrow keys or by entering the desired test number into the test number field using the numeric keys.

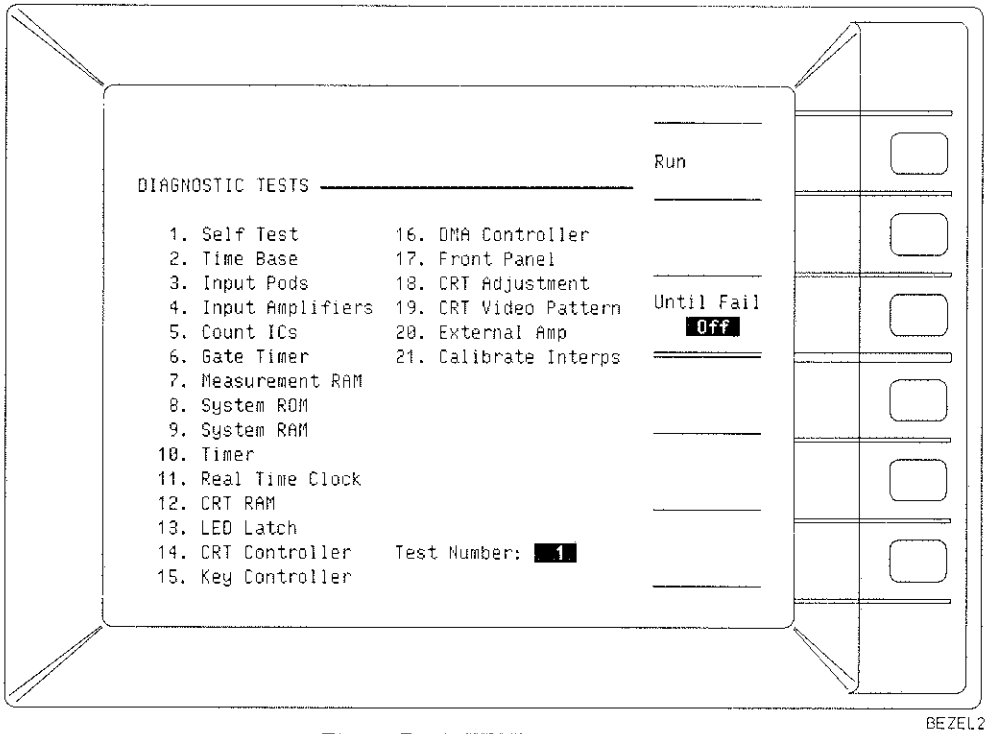


Figure 7A-1. TEST Menu Screen

7A-9. Standard Test Screen

Fifteen of the diagnostic tests listed on the TEST Menu Screen (i.e., Tests 2 through 16) display test results using the Diagnostic Test Screen. This screen displays the number of times the test is executed and the number of times the test fails. Also displayed are the "CURRENT RESULT" and "LAST FAILURE RESULT" along with the time at which the associated messages are displayed. The "CURRENT RESULT" field shows either the message returned the last time the test was executed, or an intermediate result displayed while the test is running. The Memory and Count ICs Tests display intermediate results to give more detailed failure information that can't fit into the return message. The "LAST FAILURE RESULT" field shows the message returned by the test the last time it failed. Intermediate results are not displayed in the "LAST FAILURE RESULT" field.

A test selected from the TEST Menu Screen and initiated by pressing Run softkey, is repeated continuously until the Stop softkey is pressed. If the Pause softkey is pressed while the test is running, the test pauses until the Run softkey is again pressed. The test can also be executed in "Until Fail" mode, where the test pauses when a failure occurs.

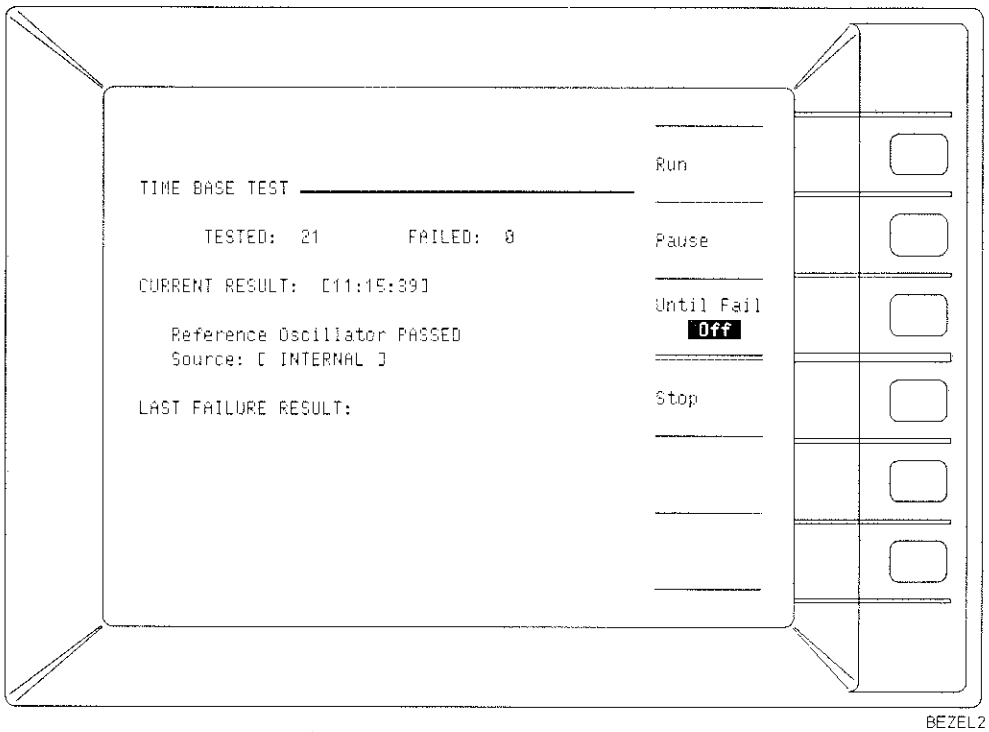


Figure 7A-2. Diagnostic Test Screen

7A-10. Test Descriptions

The following paragraphs describe each diagnostic test and lists possible messages and results.

7A-11. TEST 1. SELF TEST

The Self Tests are a series of tests that exercise various sections of the 5371A. Self Test requires no user interaction and since Measurement RAM locations are tested, is always destructive to data stored in memory.

The results of the self tests are displayed on the Self-test screen. Each test is listed on the screen, grouped by board assembly number (i.e., indicated inside brackets [1]), and is followed by PASS or FAIL indicating whether the test passed or failed. The name of the test currently being executed is highlighted on the Self-test screen. The screen also displays the message and the time of last failure associated with the last observed failure. The system keeps track of the number of times the Self-test is performed and the number of times the Self-test fails. The following tests are executed during Self-test:

- Test 2. Timebase Test
- Test 3. Input Pod Test
- Test 4. Input Amplifier Test
- Test 5. Count ICs Test
- Test 6. Gate Timer Test
- Test 7. Measurement RAM Test
- Test 8. System ROM Test
- Test 9. System RAM Test
- Test 10. Timer Test
- Test 11. Real-time Clock Test
- Test 12. CRT RAM Test
- Test 13. LED Latch Test
- Test 14. CRT Controller Test
- Test 15. Keyboard Controller Test
- Test 16. DMA Controller Test

7A-12. TEST 2. TIME BASE TEST

During this test, the 68000 μP (located on A7 Processor Board) reads a 16-bit status byte to determine the state of the 5371A timebase reference source. The test passes if both the internal 10 MHz A15 Oven Oscillator (HP Part Number 10811-60111) and 500 MHz reference frequency are locked. The return message indicates if the oscillator source is generated internally or externally (via the rear-panel EXTERNAL INPUT connector).

The status word is latched onto the Count Hardware Bus by buffer A1U31, which is located on the A1 Timebase Control Board. The status word, located at address 710030 (hexadecimal) in memory, is addressed by PAL IC A1U21 to enable A1U31. Only the lower status word byte contains actual data. The status word bits are mapped as in *Table 7A-1.*

Table 7A-1. Timebase Status Word Bit Map

Bit	Description
0	Bit 0 = 1 if External Source Present
1	Not Used
2	Bit 2 = 1 if Internal Timebase Source Present
3	Bit 3 = 0 if Phase-locked Loop is Locked
4	Not Used
5	Bit 5 = 1 if a Timebase Reference Change From Internal to External Source Occurs
6	Bit 6 = 1 if a Timebase Reference Change From External to Internal Source Occurs
7	Bit 7 = 1 if Phase-locked Loop loses lock
8-15	Contain No Usable Data

The Timebase Test examines Bit 3 to check if the A14 Timebase Multiplier Board's phase-locked loop circuit is locked. If Bit 3 is set to 1, the test passes. If, on the other hand, a 0 is detected, the test fails with the "Unlocked" failure. Bits 0 and 3 are also examined. One bit should be set to 1, while the other should be set to 0. If both are set to 1, then the test fails the "Ext & Int Source" failure. If both are set to 0, then the test fails the "No Source" failure.

Messages:

Reference Oscillator PASSED Source: [EXTERNAL]
Reference Oscillator FAILED Source: [INTERNAL] Unlocked: [10 500]

Indicates that the oscillator is not locked.

Reference Oscillator FAILED - Ext & Int Source: [EXTERNAL INTERNAL}

The status bits indicate that both an internal and external timebase reference are present. This condition should never occur. If it does, erroneous data is being sent from the status register, which is located on the A1 Timebase Control Board.

Reference Oscillator FAILED - No Source Source [ ]

The status bits indicate that neither and internal or external timebase reference are present. This condition should never occur. If it does, erroneous data is being sent from the status register, which is located on the A1 Timebase Control Board.

7A-13. TEST 3. INPUT POD TEST

This test checks for proper installation of both Channel A and Channel B Input Pods. Three ID (Identification) bits generated by each pod determine which type (i.e., HP 54001A, 54002A, or 54003A), or if any, pods are installed in the 5371A. This test passes only if pods are installed in BOTH pod locations. The type of pod installed in each location is identified in the return message. If your HP 5371A is equipped with Option 060, Rear Panel Inputs, then the input pod test is not performed.

Messages:

Pods Present - PASSED A:[54002] B:[54001]
Pods Missing - FAILED A:[NO_POD] B:[NO_POD]

Rear panel inputs installed, POD test not performed.

During the Input Pod Test, the 68000 μP reads POD ID Latch, A1U29, located on the A1 Timebase Control Board. The POD ID latch, which is located at address 710041 (hexadecimal), drives the byte of information onto the Count Hardware Data Bus. PAL IC, A1U21, decodes the address to enable A1U29.

Each input channel pod generates a 3-bit signal that is pulled to +5V through A1R95 on the A1 Timebase Control Board. Each type of pod inserted in the front panel has a unique pattern of shorting these three lines to ground. The bits for POD ID latch are mapped as indicated in *Table 7A-2*.

Table 7A-2. POD ID Bit Map

Bit	Input Pod Channel	Bit Description
0	A	LSB
1	A	Bit
2	A	MSB
3	Not Used	0
4	B	LSB
5	B	Bit
6	B	MSB

After test reads the output of the POD ID Latch, the data read is divided into two parts; one for Channel A Input Pod, and one for Channel B Input Pod. The data should correspond to the values listed in *Table 7A-3*. Any value not listed generates a "NO POD" failure.

Table 7A-3. Input Pod ID Data

ID2n (MSB)	Bits ID1n	ID0n (LSB)	Input Pod Type
1	1	0	HP 54001A
1	0	0	HP 54002A
1	0	1	HP 54003A
n = A or B, depending in which channel the pod is installed.			

7A-14. TEST 4. INPUT AMPLIFIER TEST

The Input Amplifier Test perform a series of tests on the A2 Input Amplifier Board. The description of each test follows:

a. Comparators A2U4 and U15 are tested to ensure that they will not toggle when inputs are removed from each channel. The trigger level and input bias voltages are set to 0 V on both channels. The counting hardware is programmed to count pulses generated by both comparators. If pulses are counted on either channel, the test fails.

b. The auxiliary comparator (A1U15AB) outputs are tested by forcing them low and then high. This is accomplished by setting the input biases to 0 V, then setting the trigger levels to 1 V, then –1 V. With the trigger level set to 1 V, the auxiliary comparators should indicate that the signal is below the trigger level. With the trigger level set to –1 V, the auxiliary comparators should indicate that the signal is above the trigger level.

c. The slope controls lines are tested by changing them from positive to negative. With the input bias still at 0 V and the trigger level still at 1 V, the output of the auxiliary comparators should change.

d. This test ensures that the comparators trigger on the correct number of events as detected by the counting hardware. The counting hardware is programmed to count events from the channel being tested. A forced latch is performed and the count is saved. Then, 100 pulses are generated using the signal from

the bias MUX which is controlled by the trigger level DAC of the channel not currently being tested. Approximately 100 events should be counted. A second forced latch is then performed and a second set of 100 events is counted and. added to the first set. If the difference between the two forced latches is within 15% of 100, the test passes. This test is performed once for each channel.

e. *Input Switching Test 1:* Tests relays A2K2, K3 and K4 as a unit. These relays are set up so that the input level to Channel A of the input amplifier is 1 V. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes.

f. *Input Switching Test 2:* Tests relay A2K2. Relays A2K1 and K2 are switched from the previous setup so that the input level to Channel A is 575 mV. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K2 must be at fault.

g. *Input Switching Test 3:* Tests relay A2K3. Relay A2K3 is switched from the previous setup so that the input level to Channel A is 0 V. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K3 must be at fault.

h. *Input Switching Test 4:* Tests relay A2K4. The relays are set μP so that the input level to Channel A of the input amplifier is –2 V. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K4 must be at fault.

i. *Input Switching Test 5:* Tests relays A2K6, K7 and K8 as a unit. The relays are set up so that the input level to Channel B of the input amplifier is 575 mV. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes.

j. *Input Switching Test 6:* Tests relay A2K8. Relay A2K8 is switched from the previous setup so that the input level to Channel B is 1 V. A peak search is performed on the input level and if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K8 must be at fault.

k. *Input Switching Test 7:* Tests relay A2K7. Relay A2K7 is switched from the previous setup so that the input level to Channel B is 575 mV. A peak search is performed on the input level; if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K7 must be at fault.

l. *Input Switching Test 8:* Tests relay A2K6. Relays A2K5 and K6 are switched from the previous setup so that the input level to Channel A is 1 V. A peak search is performed on the input level: if it is within 15% of the expected value, the test passes. If this test fails and the previous tests passed, relay A2K6 must be at fault.

m. *Bias MUX Test.* Tests Termination Bias Selection Multiplexers (MUXs) A2U7 and U21. Each input of the bias MUX is sent to the input channels. A peak search is performed on each of the levels to determine if they are within an acceptable range. The four MUX inputs are –2 V, 1 V, 0 V, and DAC control level. The DAC control levels are set to 2 V. The expected voltage level is 1/10 of 2 V DAC control level (200 mV). Eight tests are performed; Tests 1, 3, 5, and 7 test the –2 V, 1 V, 0 V, and DAC biases respectively for Channel A while tests 2, 4, 6, and 8 check the same voltage levels for Channel B.

When both the relay (input switching) and bias tests are complete, a message is returned indicating whether one or the other type of test has failed (or both types, if applicable).

Messages:

Input Amp Test PASSED
Input Amp Test FAILED — Input Amp Oscillating A[313] B[0]

The input amplifier is oscillating with no input signal. The number of counts detected for each channel is returned in the error message.

Input Amp Test FAILED — Bad comparator result A: Stuck High B: Stuck Low

The auxiliary comparators returned bad results. The results are returned in the error message along with the expected results in parentheses.

Input Amp Test FAILED — Slope control failed: [Channel A] [Channel B]

The input amplifier slope control failed. The results are returned in the error message along with the expected results in parentheses. Both comparators should change to the low state.

Input Amp Test FAILED — Bad Counts A[0] B[100]

An incorrect number of events was detected by the counting hardware (100 events were expected on each channel). The actual number of counts detected on each channel is returned in brackets in the error message.

Input Amp Test FAILED — Input Switching Failure

This message is returned if any of the relay tests fail.

Input Amp Test FAILED — Input Bias Failure

This message is returned if any of the bias tests fail.

Input Amp Test FAILED — Input Switching or Input Bias Failure

This message is returned if any of the relay tests or bias tests fail.

Intermediate Messages:

Input Switching Test 1: Max: 1038 (Min: 1040) [1115 1360]

If a relay test fails, an intermediate message containing the DAC result followed by the acceptable range in brackets is displayed. The minimum peak level is also searched for and returned if an error is detected.

Input Bias Test 5: Max: 2072 (Min: 2070) [2191 2235]

If a bias test fails, an intermediate message containing the DAC result followed by the acceptable range in brackets is displayed. The minimum peak level is also searched for and returned if an error is detected.

7A-15. TEST 5. COUNT ICs TEST

This test exercises the Sequencer and ZDT counter ICs which are both located on the A5 ZDT/Count Board. These hybrid ICs perform the actual event and time counting measurements of the HP 5371A. Each ZDT has an internal 16-bit counter with two 16-bit latches that are capable of latching (sampling) the contents of the counter without

disturbing the count. The Sequencer acts as traffic cop to control which signals are counted and which signals control the measurement. To test the ZDTs, the Sequencer is programmed to gate the 500 MHz reference frequency to the Event 1 and Event 2 Counter chain clock inputs. The 500 MHz signal is hard-wired to the Timing Counter ZDT chain clock input. Since the ZDTs are configured into three chains comprised of two cascaded ZDTs each, each chain can be tested separately. The ZDT are tested by the following pairs: Event Counter 1 (ZDT1A & ZDT1B), Event Counter 2 (ZDT2A and ZDT2B), and the Timing Counter (ZDT3A & ZDT3B). Each of the three ZDT chains are exercised as follows:

a. The data paths to the ZDT chain are tested. The ZDTs are preset to the value AAAA (hexadecimal). This prevents them from counting and sets the internal count value to AAAA (hexadecimal). Forced latches are then performed on Latches 1 (L11 and L21) and Latches 2 (12 and 22). The results are then read back and compared to the initial preset value. This test is then repeated for the 5555 (hexadecimal) pattern.

b. The latch status bits for Latches 1 (L11 and L21) and 2 (L12 and L22) are checked. They should be set already since the last action performed by the previous test was a forced latch.

c. The ZDTs are reset and the latch status bits are checked again. The bits should now be cleared.

d. The Terminal Count (TC) bits are tested. A reset is performed first. This clears the terminal count bits. The ZDTs are then preset to FFFF (hexadecimal). ZDTxB is then programmed to FF00 (hexadecimal) causing a carry-out from the first stage ZDTxB. This should cause the terminal count bit of ZDTxB to set. Then ZDTxA is programmed to FF00 (hexadecimal) causing a carry-out from the first stage of ZDTxA. This causes the terminal count bit of ZDTxA to set.

e. The ZDTs are tested to check their ability to count. The ZDTs are preset to 0 and then a reset is performed enabling counting. A software delay loop is executed and Latches 1 (L11 and L21) and 2 (L12 and L22) are forced. The values of the forced latches should differ from the initial preset values.

f. The latches are read a second time to see if they held the latched values. The values read the second time should match the value read the first time.

g. The enable latch function is tested. The latches are enabled, a software delay loop is executed, and Latches 1 (L11 and L21) and 2 (L12 and L22) are forced. The values read the second time should be different from the values of the latches before they were enabled.

h. Two Totalize measurements using Gate Timer, A6U41, are performed to test the accuracy of the ZDT count ICs. The 500 MHz reference frequency is routed to each of the ZDT chains. Measurements using a 4.6 us and 4.1902 ms gate times are made on each ZDT chain. The 4.6 us gate time measurement should return a result of 8FC (hexadecimal) ±3, while the 4.1902 ms gate time measurement should return a result of 1FF7FC (hexadecimal) ±3. Two measurements are made to ensure that the high and low order ZDTs are tested. The values 4.6 μs and 4.1902 ms were chosen because they have values that end with the bit pattern FC. The test is more likely to fail when there are numerous 1's in the expected pattern.

NOTE

If a test fails, a failure message is displayed. If Test H causes the ZDT being tested to lock up and no failure messages are displayed, then Tests A through G have passed.

Messages:

Count ICs PASSED
Count ICs FAILED: ZDT1A,ZDT1B,ZDT2A,ZDT2B,ZDT3A,ZDT3B

Intermediate Messages:

ZDT1A FAILED: Read bad preset value through forced latch1 RD: FFFF WR: AAAA
ZDT1A FAILED: Read bad preset value through forced latch2 RD: FFFF WR: AAAA
ZDT1A FAILED: Latch1 status bit not set after forced latch RD: FFFF WR: 0
ZDT1A FAILED: Latch2 status bit not set after forced latch RD: FFFF WR: 0
ZDT1A FAILED: Latch1 status bit set after ZDTs reset RD: FFFF WR: 0
ZDT1A FAILED: Latch2 status bit set after ZDTs reset RD: FFFF WR: 0
ZDT1A FAILED: Terminal Count not cleared after reset RD: FFFF WR: 0
ZDT1A FAILED: Terminal Count not set after 0FFFFH preset RD: FFFF WR: 0
ZDT1A FAILED: Latch1 is not changing after a reset RD: FFFF WR: 0
ZDT1A FAILED: Latch2 is not changing after a reset RD: FFFF WR: 0
ZDT1A FAILED: Latch1 is changing after a forced latch RD: FFFF WR: 0
ZDT1A FAILED: Latch2 is changing after a forced latch RD: FFFF WR: 0
ZDT1A FAILED: Latch1 is not changing after an enable latch RD: FFFF WR: 0
ZDT1A FAILED: Latch2 is not changing after an enable latch RD: FFFF WR: 0
ZDT1 chain FAILED — incorrect count total [4.6 us gate]: 7FE [8FC]

The ZDT counter ICs are tested by writing and reading patterns to each IC and comparing the patterns to expected results. The decoding for the ZDTs and Sequencer is performed by PAL IC A6U17 located on the A6 DMA/Gate Board. The ZDTs are connected directly to Event 1 & 2 and Timing Counter Measurement RAMs, and to numerous bus buffers. These bus buffers are controlled by PAL IC A6U36, also located on the A6 DMA/Gate Board.

If all ZDTs indicate a similar failure mechanism, the cause may be something other than the ZDTs. If the patterns "AAAA" and "5555" are incorrect, a bit located either on the Count Hardware Data Bus or the A5 ZDT/Count Board could be stuck. If data read is "FFFF", the ZDT buffers may not be enabled. Check PAL ICs A6U17 and U36.

NOTE

Test 7, Measurement RAM Test, also tests the ZDT buffers. Therefore, if Test 7 passes, the ZDT buffers should be operational.

Tests E and H check the ability of the ZDT counter chains to count. If Tests E and/or H fails, the ZDTs may not be receiving the 500 MHz reference frequency. No clock or wrong clock frequency could cause Tests E and H to fail.

Test H uses the System Gate Timer IC (A6U41) and count hardware control circuits. If all three ZDT chains fail or lock up, check these circuits. Remember that the System Gate Timer Test, Test 6, does not test the TTR, TG1, or TG2 signal paths. Test H uses the double-latch setμP in the Count hardware control circuits.

7A-16. TEST 6. GATE TIMER TEST

This test exercises the Gate Timer IC, A6U41, located on the A6 DMA/Gate Board. The Gate Timer IC generates the intervals for used during Time Interval measurements. A6U16 decodes the 68000 μP address that enables the Gate Timer. Transceivers A6U57 and U58 buffer the data from the Count Hardware Data Bus onto the A6 DMA/Gate Board's data bus. Flip-flops A6U59AB divide CLK10 (10 MHz) by two, providing the Gate Timer IC with a 5 MHz timebase and a signal to disable the clock during programming. Latch A6U42A synchronizes the TTR edge to the 5 MHz clock. Latches A6U42B and U32 generate a pulse when TTR is first received. The Gate Timer IC generates the pulses at the programmed interval after TTR is received.

The data path to the Gate Timer is tested first by writing and reading AAAA (hexadecimal) and 5555 (hexadecimal) to an internal register. In both cases, the pattern read back should be the same. If either of these two tests fail, the Gate Timer IC or the data path may be suspect. Since the Interpolator RAMs use the same data path, performing and passing Test 7, Measurement RAM Test, will verify that the data path is OK. If a failure is detected, check all buffers in the data path. They include A6U19A, U22, U57, U58, U13, and U18.

Next, the two timers within the Gate Timer are tested. This test loads the Gate Timer's internal counters with an initial value, 200000, and allows them to count down for a set period of time (approximately 10 ms as determined by software). The new count value is latched into the IC's hold register and compared with an expected value of about 100000. If the latched count is within 11% (±11000) of the expected value, the Gate Timer passes the test. The latched count is included as part of the return message. If only one of the internal gate timers fails, then the IC is probably defective. If both gate timers are defective, giving similar counts, then maybe some support circuitry may be defective. If the 5 MHz Gate Timer timebase is off, then this test will fail. Also, if a circuit problem in another part of the 5371A is generating a 68000 μP interrupt, the microprocessor may not have time to count the 10 ms correctly, resulting in an incorrect count.

NOTE

The following two items not tested by Test 6, Gate Timer Test:

1. Time TRigger (TTR) signal path from the Sequencer (A5U29) to the Gate Timer (A6U41) is not tested.
2. TG1 and TG2 Gate Timer signal paths from the Gate Time (A6U41) to the Sequencer (A5U29) are not tested.

Messages:

Gate Timer 1 PASSED: count=[100000] Gate Timer 2 PASSED: count= [100000]
Gate Timer FAILED W: AAAA R:FFFF

If the data path test fails, the values that were written and read are returned in the error message.

Gate Timer 1 FAILED: count = [200000] Gate Timer 2 FAILED: count = [0]

If the latched count is not within the acceptable range, the test fails and the bad count is included in the return message.

7A-17. TEST 7. MEASUREMENT RAM TEST

NOTE

The Measurement Ram Test always destroys data stored in memory regardless of whether it is run at power-up, from diagnostics, or via HP-IB.

This test exercises the measurement RAM ICs used to store data output by the ZDT counters and the Interpolators. The ZDT counter output is stored on the A5 ZDT/Count Board and the Interpolator output is stored on the A6 DMA/Gate Board. These RAMs are 8-bit devices while the ZDT counters and Interpolators are 16-bit devices. Therefore, each ZDT counter has two RAMs in which to store its latch data output. The Measurement Ram Test exercises both RAMs associated with each ZDT counter at the same time. This test is always destructive to data whether the test is run at instrument power-μP or from the Diagnostics menu.

The RAMs are tested by writing and reading patterns to each memory location and comparing these patterns to expected results. The addresses for each RAM location are generated by the "DMA Measurement RAM Address Generation" circuit's RAM address counters (A6U9 through A6U12) located on the A6 DMA/Gate Board. Also located on the A6 assembly is Memory PAL IC (A6U16) that enables the RAM Output Enable (~RAMOE) for all the measurement RAMs during a read cycle. The latches that buffer each set of RAMs from the data bus are controlled by the Buffer PAL IC (A6U36) also located on the A6 assembly.

The test begins with the two RAMs associated with counter ZDT1A. Hexidecimal AAAA is written to all measurement locations. Next, the first memory location is read. If AAAA (hexadecimal) is not read, the test fails and ends. If data read is OK, 5555 (hexadecimal) is written to the first memory location. Next, the memory location is read. If 5555 (hexadecimal) is not read, the test fails and ends. If the data read is OK, then 8888 (hexadecimal) is written to the first memory location. This checks for uniqueness at all RAM locations. The test just described is repeated for all memory locations.

If all the measurement RAMs fail in a similar fashion, the problem could be caused by something other than the RAMs being tested. If the patterns AAAA and 5555 are incorrect, check the Count Hardware Data Bus path on the A5 ZDT/Count, A6 DMA/Gate, and A12 Motherboard. If all the RAMs read back 8888 instead of AAAA, then the RAM Address Counters (A6U9 through A6U12) or the RAM Address Latches (A5U1 and U5, A6U28 and U30) could be defective. If all the data read back is FFFF, then the buffer ICs that buffer the RAMs may not be enabled. Check Buffer PAL IC, A6U36. Also check the Memory PAL IC, A6U16, for RAM Output Enable (~RAMOE) activity.

If only one set of RAMs fails, then the RAMs or the associated ZDT counter could be suspect. If the ZDT counter is installed incorrectly or has an output that won't toggle, the test might fail. Check each pair of latches, or buffers, for proper control signals.

Messages:

Measurement RAM PASSED
Measurement RAM FAILED: 1A 1B 2A 2B 3A 3B INT

A list of the failed measurement RAMs is returned.

Intermediate Messages:

Measurement RAM 1A [Fail]: 800 W: AAAA R: 8888

If a measurement memory failure is detected, the address at which the failure occurs and the data that was written and read are displayed in the intermediate message.

7A-18. TEST 8. SYSTEM ROM TEST

The System ROMs located on the A7 Processor Board are tested by performing a checksum on each ROM.

Messages:

System ROM PASSED
System ROM FAILED: U45 U44 U49 U48 U51 U50

A list of System ROMs that fail the checksum test is returned.

Intermediate Messages:

System ROM U28 [Fail] Sum = 582E2A [593FB2]

If an incorrect checksum is detected, the measured checksum value and the expected checksum value (in brackets) are displayed in the intermediate message.

7A-19. TEST 9. SYSTEM RAM TEST

The System RAM ICs located on the A7 Processor Board are tested by writing and reading hexadecimal bit patterns (AA and 55) to and from each 8-bit memory location. This test is non-destructive to the data stored in System RAM when the test is run from the TEST menu. The current data stored in each memory location is stored prior to testing that memory location. Following the test of each memory location, the original contents of the memory are restored.

But when this test is performed during the instrument power-up sequence, a destructive test that establishes a unique relationship between memory locations is performed. All memory locations are preset to hexadecimal AA, read, set to 55, read, and set to 88. If any two memory locations are mapped to the same memory location, bit pattern 88 is read instead of the expected AA.

Messages:

System RAM PASSED
System RAM FAILED: U45 U44 U49 U48 U51 U50

A list System RAM ICs that fail is returned.

Intermediate Messages:

System RAM U45 [Fail]: 1E72 W:AA R:88

If a memory failure is detected, the address at which the failure occurred and the data written to that location are displayed in an intermediate message.

7A-20. TEST 10. TIMER TEST

A counter located within Program Timer (A7U13) is set to count down to zero and then preset to an initial value of 20000. A software loop then programs the counter to count for approximately 10 milliseconds. After the 10 millisecond count period, the current value stored in the counter is latched and compared with an expected value. If the value is within an acceptable range, ±11 %, the timer passes the test. The latched count value is returned as part of message.

Messages:

Timer PASSED count = [10000]
Timer FAILED count = [0]

If the latched count is not within the acceptable range, ±11%, the test fails and the bad count is included in the return message.

7A-21. TEST 11. REAL-TIME CLOCK TEST

This test checks the tenths-of-a-second register of the Real-time Clock IC (A7U46) to ensure that it is incrementing. The number of times the wait loop is executed before a change in the tenths register is detected is included in the return message.

Messages:

Real Time Clock PASSED: Count = [245] 21 Aug 1987 09:54:55
Real Time Clock FAILED: Not Responding - Timeout Occurred.

If a change in the tenths register is not detected within the timeout period, the "Not Responding" error message is returned. The two bracketed numbers that precede the count are the contents of the tenths register before and after executing the wait loop.

Real-time Clock FAILED: Non-consecutive Increment [1] [3] Count = [244]

If the value of the tenths register changes by an amount other than +1, the "Non-consecutive Increment" error message is returned. The two bracketed numbers that precedes the count are the contents of the tenths register before and after executing the wait loop.

7A-22. TEST 12. CRT RAM TEST

The CRT Display RAM ICs (A8U15, U19, U23, and U27) are located on the A8 I/O Controller Board. This memory, which stores the bit-mapped front-panel CRT Display image, is tested by writing and reading hexadecimal bit patterns A and 5 to and from each 4-bit memory location. Each word of CRT Display Memory is stored in four 4-bit wide RAMS. This test checks each Display RAM IC individually.

This test is non-destructive to the data stored in Display RAM if the test is run from the TEST menu. The data currently stored in each memory location is stored prior to testing that memory location. Following the test of each memory location, the original contents of the memory are restored.

This test is destructive to memory if performed during the instrument power-up sequence since the test establishes a unique relationship between memory locations. All memory locations are preset to hexadecimal AA, read, set to 55, read, and set to 88. If any two memory locations are mapped to the same memory location, bit pattern 88 is read instead of the expected AA.

Messages:

CRT RAM PASSED
CRT RAM FAILED: U19 U15 U27 U23

CRT Display RAM ICs that fail the test are returned with the error message.

Intermediate Messages:

CRT RAM U19 [Fail]: 0 W: A R: FF

If a memory failure is detected, the address at which the failure occurs, and the data that was written to and read from are displayed with the intermediate message.

7A-23. TEST 13. LED LATCH TEST

Two unique bit pattern, 10101010 and 01010101, are written and read from the 8-bit LED Latch, A8U9. The test passes only if the data written matches the data read.

Messages:

LED Latch PASSED
LED Latch FAILED W: AA R:FF

7A-24. TEST 14. CRT CONTROLLER TEST

The CRT Controller IC (A8U12) is located on the A8 I/O Controller Board. The CRT Controller Test verifies that the CRT Controller is active and receiving commands. Data is written and than read from one of the IC's cursor registers. Bit patterns 10101010 and 01010101 are written and read from the controller. If the test fails, the bit patterns that were written and read are displayed in hexadecimal format in the return message.

If the CRT Controller is failing, the front-panel CRT can not function properly since the proper horizontal and vertical synchronization signals are not being received. Another possible cause for failure is the dynamic CRT Display RAM ICs (DRAMs) are not being refreshed. The 5371A will still power-up but will be unable to make measurements properly.

Messages:

CRT Controller PASSED
CRT Controller FAILED W: AA R: FF

7A-25. TEST 15. FRONT PANEL KEYBOARD CONTROLLER TEST

The Front Panel Keyboard Controller IC (A8U1) is located on the A8 I/O Controller Board. This test checks the data path to the controller and verifies activity and that it can respond to commands. Hexadecimal bit patterns AA and 55 are written to and then read from the match-value registers of the controller IC.

To write data to the controller, a "write" command followed by the data is sent to the controller. To read the data back, a "query" command is sent to the controller. When the controller is ready to be read, it sends an interrupt to the 68000 μP. The microprocessor now reads the data from the controller's data buffer.

Messages:

Front Panel Controller PASSED
Front Panel Controller FAILED Front Panel Controller Not Responding

Prior to sending a command to the front panel, the instrument's software waits for the controller to set the status register bit 1 to 0. If this doesn't occur within the timeout period, the above "Not Responding" error message is returned.

Front Panel Controller FAILED Front Panel Controller Not InterrμPting

When reading a parameter from the controller, the instrument's software sends the controller a query command and then waits for it to send an interrupt back to the 68000 μP. The data is then read from the controller's data register. If the interrupt is not generated within a timeout period, the "Not Interrutping" error message is returned.

Front Panel Controller FAILED W: AA R: 00 W: 55 R: 00

If the incorrect bit pattern is read from the controller, the data written and read are displayed in the error message.

7A-26. TEST 16. DMA CONTROLLER TEST

The DMA Controller IC (A8U30) is located on the A8 I/O Controller Board. The data path to controller is tested by writing and then reading hexadecimal bit patterns AAAA and 5555 to the IC's Channel 0 Current Address Register. The controller is then functionally tested by exercising it in "verify" mode. In this mode, the DMA Controller IC performs a DMA transfer with the measurement memory and I/O lines inactive. NO data is actually transferred.

In the "verify" mode, the DMA Controller is set up to "transfer" 10 bytes on Channel 1. The transfer is started and the test enters a loop that polls the status of the DMA Controller. If the transfer is not completed within a certain time, the loop is exited and a failure message is returned. If the transfer is completed, the actual count is read from the controller and should equal –1. The address is then read from the controller and should be 11. The controller passes this test only if both conditions are true.

Messages:

DMA Controller PASSED
DMA Controller FAILED W: AAAA R: EAAA

If the test of the data path fails, both the value that was written and read are returned in the error message.

DMA Controller FAILED: Not Responding

If the DMA Controller does not indicate that the test transfer is complete within a specified timeout period, the "Not Responding" error message is returned.

DMA Controller FAILED: Bad Count [0]

Following the test transfer, the byte count should equal –1. If not, the "Bad Count" error message is returned along with the contents of the count register.

DMA Controller FAILED: Bad Address [0]

Also following the test transfer, the current address register should be 11. If not, the "Bad Address" error message is returned along with the contents of the current address register.

DMA Controller Test STOPPED

This message is returned if the DMA Controller test never has a chance to run before a STOP command is received. This situation could occur if the HP-IB is tying up the DMA Controller. This test returns a PASSED status even though the test was never executed.

Intermediate Messages:

DMA Controller busy, waiting...

If the HP-IB is being used, an intermediate wait message is displayed

7A-27. TEST 17. FRONT PANEL TEST

This test allows the user to check the front-panel keypad and Rotary Pulse Generator [RPG or Data Entry Knob (DEK)]. A graphical representation of the 5371A front panel is displayed on the CRT with each keypad location highlighted. When a key is pressed, the corresponding location on the CRT turns off. When the RPG is rotated either clockwise or counterclockwise, the corresponding directional arrow on the CRT turns off. The Front Panel Test passes only after all keys have been pressed and the RPG has been rotated in the clockwise and counterclockwise directions. The test is aborted if no key depressions or RPG rotations have been detected within approximately 10 seconds. The 68000 μP-controlled LEDs are also illuminated for a visual check.

7A-28. TEST 18. CRT ADJUSTMENT PATTERN

A pattern is displayed to assist in the adjustment of the CRT. Lines marking the border of the active display area and the vertical and horizontal centers of the screen are displayed. Two solid rectangles are displayed, one at full-bright and one at half-bright intensity. These rectangles assist with the brightness adjustments. The pattern is displayed until any front-panel key is pressed.

7A-29. TEST 19. CRT VIDEO PATTERN

A pattern of alternating full-bright and half-bright vertical lines is displayed on the CRT. Each line is one pixel wide, separated from the next pixel by a space one pixel wide. Each line runs from the top to the bottom of the display area.

7A-30. TEST 20. EXTERNAL AMPLIFIER TEST

This test monitors the output of comparator A6U43B of the "External Input Amp" circuit located on the A6 DMA/Gate Board. A simulated scope waveform indicating whether the comparator is set high or low is shown on the CRT. The test runs until the user presses the STOP key.

7A-31. TEST 21. INTERPOLATOR CALIBRATION ROUTINE

This routine aids in the calibration of the A4 interpolators. The A5 Sequencer IC, A5U29, is programmed so that the interpolator trigger outputs are driven by the Channel A input signal. 800 samples are taken and stored in the A6 Interpolator Ram. A part of this data is processed and displayed graphically on the CRT Display.

When the frequency of the signal coming in on Channel A approaches a multiple of the 500 MHz reference frequency, the data read from the interpolators stabilizes. To calibrate the interpolators, a signal is selected so that the data changes slowly. When this data is shown graphically, it appears as a stair-step pattern. The interpolator stages are adjusted so that all the steps in the stair-step pattern are the same. Vertical reference lines are displayed to mark the

expected length of the stair-step pattern. These lines can be switched on and off by pressing the **GRID ON/OFF** softkey.

By pressing the **AVERAGE ON/OFF** softkey, the above routine is put into an averaging mode that displays the average lengths for the last 10 measurements. The data used in the averaging comes from the first set of data that cycles from zero through nine. The averaging feature permits a more stable display making it easier to make fine-tuned adjustments to the interpolator stages.

This test is performed on both Interpolator 1 (Start) and Interpolator 2 (Start) on the A4 assembly. When the routine is run, data patterns from Interpolator 1 (Start) are shown first. Pressing the **INTERP 2** softkey displays the data patterns generated by Interpolator 2 (Stop).

7B A1 TIMEBASE CONTROL/ A14 TIMEBASE MULTIPLIER

SECTION 7B
A1/A14 TIMEBASE CONTROL/MULTIPLIER

7B-1. A1 TIMEBASE CONTROL BOARD

7B-2. Introduction

The main functions of the A1 Timebase Control Board include the buffering, detection, and selection of either the 1, 2, 5, 10 MHz external timebase input (via the HP 5371A rear panel) or the internal A15 Oven Oscillator; provide over-voltage detection for both Channel A and B inputs; inform the 68000 μP of the installation and variety of input pods installed in the HP 5371A; and, support the A14 Timebase Multiplier, which generates the 500 MHz reference frequency, buffered 10 MHz rear-panel output, and the 125 MHz DMA clock for the A5 ZDT/Count Board's Ram Write circuit.

One of two timebase reference sources provide the signal used for generating the 500 MHz reference frequency which is used in the measurement process of the counter. One source, the high stability A15 Oven Oscillator (10811-60111) is mounted inside the HP 5371A. The A15 oscillator plugs into connector A12XA15 of the A12 Motherboard. Power to the oscillator's crystal is provided by the "Internal Timebase Control" block located on the A1 Timebase Control Board. (If a 1, 2, 5, or 10 MHz signal is not applied to rear-panel EXTERNAL INPUT connector, +15 Vdc (+15OSC) is a sent from A1 to the input of +12-volt regulator, A12U8, located on the A12 Motherboard. The regulator sends +12 Vdc to the A15 oscillator's crystal which generates a 10 MHz output. Unregulated +25V is applied to the local "+21V Oven Regulator" (A12U11), which is located on the A12 Motherboard, and whose +21V output provides the power required by the oscillator's oven heater. The oven maintains the A15 internal timebase crystal at a constant controlled temperature that ensures an extremely accurate frequency reference source whenever an external source is NOT available.

7B-3. Internal Timebase Buffer Stage

The A15 Oven Oscillator's 10 MHz output is routed via the A12 Motherboard, to the A1 assembly. The passive components terminate the 10 MHz signal while diodes A1R22 and CR23 clip it to less than approximately 1-1.5 V p-p. Comparator A1U24B translates the 10 MHz signal into an ECL level signal. From here the signal is routed to both the 10 MHz Multiplexer and the Internal Timebase Detect stages of the A1 assembly.

7B-4. External Timebase Buffer Stage

If the user wishes to use an external signal as the instrument's timebase, this signal can be applied through the rear panel connector labeled "EXTERNAL INPUT". The circuitry is identical to that of the "Internal Timebase Buffer". The external reference signal is routed from rear-panel connector A13J2, through coaxial cable W3 to the A12 Motherboard, and to the A1 Timebase Control Board connector P1. The circuit terminates, clips, and translates the external reference signal input to an ECL level. The output of this stage is sent to the "10 MHz Multiplexer" and the "External Timebase Detect" stages of the A1 assembly.

7B-5. External Timebase Detect Stage

After the external reference signal is buffered, the output of A1U24A (pin 2) is converted to a TTL level by A1U25D, and routed to the "External Timebase Detect" stage. This stage is a retriggerable, monostable multivibrator (A1U13A). The "ON" time of multivibrator is such that its output is a logical "one" as long as an input signal of appropriate period length (greater than approximately 1 μS) is connected to the HP 5371A rear panel. When external reference input signal's frequency is too low or is removed, A1U13A (pin 13) toggles low. This process monitors the presence of a signal at rear-panel connector EXTERNAL INPUT (1,2,5,10 MHz). The output of A1U13A serves two purposes:

1. Provides TTL level signal EXTPRES that informs the A7 assembly's 68000 μP that an external frequency is present at the rear panel. Also, EXTPRES is buffered and inverted by Schmitt-trigger inverter A1U7E, level-shifted to ECL level by resistive network A1R26, R27, and R28, and used to enable the external reference channel of the "10 MHz Multiplexer" stage (see "10 MHz Multiplexer" for detailed theory).

2. Provides a TTL level control signal to the Internal Timebase Control stage of the A1 assembly which serves as a switch to the crystal oscillator located inside the A15 Oven Oscillator (see "Internal Timebase Control" for detailed theory).

7B-6. Internal Timebase Control Stage

The internal timebase control stage turns A12 Motherboard +12-volt regulator A12U8 on and off, which supplies +12 Volts to the A15 Oven Oscillator's crystal. Transistors A1Q2 and Q6 provide a switchable +15 Volts to regulator A12U8. If an external reference signal is present at the rear-panel connector, DC power to the crystal is turned off. The A15 oscillator's internal oven is connected to the regulated +21V so remains on even when the front-panel STBY-ON switch is in the STBY position. This keeps the internal A15 circuitry stable while shutting off the 10 MHz output and preventing interference.

7B-7. Internal Timebase Detect Stage

One output of comparator A1U24B (pin 14) passes through ECL-to-TTL translator A1U25C, and to the input of latch A1U13B (pin 9). This circuit generates a signal, INTPRES, that is used by A7's 68000 μP for diagnostic purposes. Annunciator LED A1DS1 gives a visual indication of the internal timebase's status (on or off).

7B-8. 10 MHz Multiplexer Stage

This stage selects either the A15 10 MHz internal timebase (10811-60111) or the source that's connected to the rear-panel EXTERNAL INPUT connector. Selection is based on what the External Timebase Detect circuit sees. If a signal is detected at the EXTERNAL INPUT connector, the HP 5371A automatically uses it as a reference. Selection of either the internal or external reference source is not therefore controlled directly by the user. Instead it is controlled by applying or removing the frequency source from the rear panel EXTERNAL INPUT connector.

One of the two reference sources is selected by NOR gates A1U12B and U12C, buffered by NOR gate U12A, and routed to the "Divide-By-N" stage.

7B-9. Divide-By-N Stage

This stage divides either the internal or external reference signal by 1, 2, 5, or 10 with the objective of always generating a 1 MHz input for the A14 Timebase Multiplier. This occurs whether the external reference source is 1, 2, 5, or 10 MHz. The A1U11 divider is controlled by a 3-bit digital signal from shift register A1U23 located in the "N Control" stage. Timer A1U10 clocks shift register A1U23, which cycles through all possible combinations, but whose output is tapped in such a way to allow A1U11 divider to divide by 1, 2, 5 or 10 only.

The time required to update the "N Control" stage is less than that required by the A14 Timebase Multiplier circuits to lock onto the 1 MHz output of the "Divide by N" stage. The VCO tuning voltage [or out-of-lock voltage (VT500)] from the A14 Timebase Multiplier circuits, is routed through a window comparator stage (U22AB) that checks to see if VT500 is between +1 and +9 Vdc (nominal). The window comparator sends a control bit (INTLOCKED) to A7 assembly's 68000 μP for diagnostic purposes, and sends a control line to the "N Control" stage to turn timer A1U10 on and off.

The following is an example of how the circuitry operates. Assume that the A14 Timebase Multiplier is out-of-lock, a condition that could exist when the HP 5371A STBY-ON switch is turned to ON position or when an external reference source is connected to the rear-panel EXTERNAL INPUT connector. The A1 "Divide-By-N" stage is probably not providing the A14 phase-locked loop circuit with a 1 MHz reference input. The window comparator,

located on the A1 Timebase Control Board detects an out-of-lock status. This enables the "N Control" stage. A1U23 begins sequencing through all possible combinations. Divider A1U11 begins sequentially to divide the reference frequency by 1, 2, 5, and 10. Eventually a 1 MHz reference output will be generated, assuming of course that the reference input is either 1, 2, 5, or 10 MHz. Enough time is allowed before the "N Control" divide ratio is changed for the A14 Timebase Multiplier to lock on to the 1 MHz signal. When locked on, tuning control voltage, VT500, will fall within the +1 to +9 Vdc window. The window comparator (A1U22AB) turns off the "N Control" stage, stopping the sequencing at the correct division ratio and maintaining the 1 MHz output.

7B-10. Reference Output Buffer Stage

This stage takes a 10 MHz ECL-level output from the A14 Timebase Multiplier assembly, routes it through ECL-to-TTL translator A1U25AB, buffers and generates the rear-panel 1 V p-p 10 MHz square wave output capable of driving a 50-ohm load. This stage also generates a 10 MHz signal, CLK10, that is used to clock the A6 DMA/Gate "System Timing Controller" (A6U41) circuitry.

7B-11. A2 Input Amplifier Board Support Circuitry

7B-12. Overload Sense Stage — Channels A and B

The overload sense stages of both Channels A and B, in conjunction with their respective overload latch stages, monitor the analog input voltage levels and provide the control signals that open the A2 relays when an over-voltage condition is detected. Channel A and B input signals are monitored through resistive dividers; A2R19-A1R11 for Channel A inputs, and A2R83-A1R44 for Channel B inputs. These sense lines, OVER V A and OVER V B, are routed to their own window comparator: A1U4AB (Channel A), and A1U16AB (Channel B). The voltage window for Channel A is set by resistors A1R9 through A1R12. Similarly, Channel B's voltage window is set by resistors A1R42 through A1R45. The window comparators detect when the input signal exceeds approximately ±2.7 Volts. The status of both window comparators is latched by their respective Overload Latch stages.

7B-13. Overload Latch Stage — Channels A and B

This circuit latches the overload sense stage window comparator outputs. It then alerts the A7 68000 μP by generating a control bit that sends an interrupt (~INT3) and contributes to the pod status byte. When an over-voltage condition is detected, the respective channel's overload latch circuit generates a signal (OVER VOLT A and OVER VOLT B) that is fed back to the A2 Input Amplifier Board's "Path Selection" stage. The A2 assembly has a hardwire-override circuit, A2U28, that opens the relays without software intervention. After the relays open, an error message is displayed on the CRT informing the user that an over-voltage condition exists. The user must physically clear the over-voltage condition and press the front-panel RESTART key to clear the error message and restart the measurement process.

7B-14. Pod Identification Latches

Each type of input pod (i.e., HP 54001A, HP 54002A, or HP 54003A) generates a unique electrical "footprint". This electrical "footprint" is routed from each pod, through cables W23 or W24 to the A12 Motherboard, and on to the A1 Timebase Control Board. This 3-bit digital signal's final destination is A1U29 of the A1's "Pod Identification Latch" stage. These signals are not strictly TTL level signals: each line is open (locally pulled up) for a logical high, and shorted (to ground) for a logical low. Both Channel A and Channel B Pod I.D. signals, ID0A-ID2A and ID0B-ID2B respectively, inform the A7 68000 μP as to what type of pod is installed. Also, ICs U18AB, U19AB, and U20D notify the microprocessor when a pod is not installed or removed from its slot while the instrument is turned on, by generating an ~INT2 interrupt signal.

7B-15. Auxiliary Comparators Stage

ICs U15AB allow the A7 68000 μP to monitor the signals at the output each input channel's comparator (A2U4 and A2U15). Both ICs are located on the A2 Input Amplifier Board.

7B-16. Address and Control Decoding Stage

PAL IC A1U21 and demultiplexers A1U27 and A1U28 provide the A1 Timebase Control and A2 Input Amplifier Boards with the necessary control and address lines. Signals such as MISC CLK, RELAY CLK, and DAC1 through DAC4 provide direct control of A2 Input Amplifier circuits. These signals are described as follows:

- MISC CLK — Provides clock to latch A2U16 that latches data from Count Hardware Data lines (CTD0-CTD7). Control bits program the termination bias, ±trigger slope, and trigger light enable for both input Channels A and B.

- RELAY CLK — Provides clock to latch A2U16 that latches relay control data from Count Hardware Data lines (CTD0-CTD7). Control bits program relay driver A2U26 which directly drives relays A2K1 through A2K8.

- DAC1-DAC4 — Provides chip select signals (~CS) for both Channel A and B trigger level control DACs A2U20 (Channel A) and A2U30 (Channel B).

NOTE

DAC1 and DAC3 signals are not currently used.

7B-17. Input Pod Power Supplies

The A1 Timebase Control Board supplies regulated ±10 Volts to both Channel A and B input pods. +15 Volts is stepped down and regulated to +10V (Channel A) and +10V (Channel B) by regulators A1U26 and A1U14, respectively. Similarly, –15 Volts is stepped down and regulated to –10V (Channel A) and –10V (Channel B) by regulators A1U33 and A1U1, respectively. The resultant ±10VA and ±10VB power supply lines are routed from A1 assembly, through the A12 Motherboard and W23 or W24 cable assemblies, and to the input pods.

7B-18. Interrupt and Status Word Processing Stage

This stage allows the A7 68000 μP to read the status of key timebase signals such as EXTPRES and INTPRES. The microprocessor must be notified when the reference frequency source changes from the internal A15 Oven Oscillator to the rear-panel EXTERNAL INPUT connector, or vice versa. ICs A1U8AB A1U9B generate an ~INT2 interrupt whenever the frequency source changes or whenever the A14 Timebase Multiplier's phase-locked loop is out of lock. The ~ROBIRD signal is the read enable for latch A1U31. When this line is asserted, the 68000 μP is reading A1U31 output lines CTD0 though CTD7.

7B-19. A14 TIMEBASE MULTIPLIER

7B-20. Operation Overview

The A14 Timebase Multiplier Assembly is basically a phase-lock loop (PLL) with an output buffer stage that operates in conjunction with the A1 Timebase Control Board to generate the 500 MHz reference frequency. The 1 MHz input frequency to the PLL is derived on the A1 assembly from either the internal 10 MHz oscillator or a 1, 2, 5, or 10 MHz external reference source. The PLL's loss-of-lock detection circuit is also located on the A1 assembly. In addition to the 500 MHz clock generation, the A14 Timebase Multiplier produces the rear-panel 10 MHz frequency standard and the 125 MHz ECL clock used for various count hardware functions.

The 500 MHz Phase-locked Loop (PLL) is operating correctly when the 500 MHz voltage controlled oscillator (VCO) is locked to the 1 MHz reference frequency — effectively multiplying the 1 MHz by 500. The A1 derives the 1 MHz PLL input by dividing either the internal or external reference frequency by either 1, 2, 5, or 10. The result of the division should always be 1 MHz. The value of the divisor is selected by successively incrementing the divisor until the A1 loss-of-lock window comparator (A1U22AB) detects lock. At this point, the divisor is frozen.

7B-21. Phase Comparator

A14U6 is an ECL-compatible phase comparator that determines the "lead" or "lag" relationship between the leading edges of the waveforms present at input pins R (1 MHz input) and V [VCO/N input]. An internal feedback connection retains the previously established relationship between the input signals at pins R and V; whether input R was leading or lagging input V.

Operation of the phase comparator may be illustrated by assuming two waveforms, R and V, of the same frequency but differing in phase relationship. The IC's internal logic establishes that signal R is leading V. The ~U output (pin 3) produces a negative pulse width proportional to the phase difference, while the ~D output (pin 12) remains high. Similarly, if V is leading R, a negative pulse is generated at the ~D output (pin 12) and a constant high appears at the ~U output (pin 3). When the signals at pins R and V are in phase (locked), both outputs ~U and ~D are high.

7B-22. Loop Filter

The loop filter, a circuit comprised of an RC filter and a low-pass active filter, determines the operating characteristics of the PLL. Phase error information is contained in the phase comparator's output duty cycle. By integrating or passing the both outputs through an RC low-pass filter comprised of A14R12-C13 and A14R13-C12, usable analog phase information for the voltage-controlled oscillator (VCO) is developed. The two phase comparator outputs, which are both normally high, differentially drive operational amplifier A14U9.

The loop filter generates a DC tuning voltage that's used by the A1 Timebase Control Board for lock detection and by the 500 MHz VCO for tuning the PPL over an approximate range of 450-550 MHz.

7B-23. 500 MHz VCO

The 500 MHz VCO is a common-base, Clapp-type LC oscillator comprised of components A14Q1, L5, C101, C102, and CR4. Capacitors C101 and C102, which compensate for parasitic capacitance, are implemented by etching parallel areas of copper on adjacent layers of the printed circuit board.

Tuning of the VCO is accomplished by varying the DC tuning voltage from the loop filter stage being applied to varactor A14CR4. The range of the tuning voltage during lock is between +1 and +9 Vdc. When the PLL is out-of-lock, loop filter could saturate causing the output of U9 to go to -10 Volts. Clamping diode A14CR5 prevents the VCO input from going more negative than approximately -0.3 Volts.

Inductors A14L3 and L5 decouple the ±10-volt power supplies from the tank circuit. At 500 MHz, A14L3 and L4 provide high impedance. Capacitors A14C19 and C20 provide DC isolation and have no affect on circuit tuning.

The tank circuit is tapped at the collector of A14Q1 and routed to differential amplifier A14U7. One input of A14U7's differential input is grounded within the IC itself. Pins 5 and 8 are collector outputs (500 MHz) while pin 7 is a bias point. A14R20 and R23 are collector resistors. Pin 5 output (500 MHz) is coupled through A14C21 to the "Output Buffer" stage. 500 MHz is the main A14 Timebase Multiplier output, and after buffering, is sent to both the A4 Interpolator and A5 ZDT/Count assemblies. A14U7 pin 8 output is routed to common-base buffer A14Q2. This circuit provides reverse isolation to the noise generated by the "Divider Chain" stages that follow. This isolates noise from the 500 MHz routed to the "Output Buffer" stage. Capacitors A14C14, C15, and diodes A14CR2 and CR3 provide DC isolation between A14Q2, which has a collector bias voltage of +10 Volts, and the "Divider Chain" stage, which operate at ECL voltage levels. A14R9 and R10 form a DC bias network and provide 50-ohm termination at the input of A14U5.

7B-24. Divider Chain Stage

The buffered output of the 500 MHz VCO enters the "Divider Chain" stage at A14U5, a wideband divide-by-two IC. This IC has two 250 MHz ECL outputs. Pin 3 is terminated into 50 Ohms by A14R6 and C9 and continues on to pin 9 of A14U2. A14U2 divides the 250 MHz by two and routes the resulting ECL-level 125 MHz (DMA CLK) through connector J8 to the A5 ZDT/Count Board's Ram Write circuitry. A14U5's other ECL-level 250 MHz output (pin 2) sequentially passes through A14U3 (divide-by-five), A14U1 (divide-by-five), and A14U4 (divide-by-10). The resulting 1 MHz output (A14U4 pin 2) is sent back to phase comparator A14U6 pin 9 for comparison with the 1 MHz reference generated by the A1 Timebase Control Board.

The frequency output of IC A14U1 is an ECL-level 10 MHz signal. Besides continuing on within the divider chain of the PLL, the 10 MHz is routed through connector J5, to the A1 Timebase Control Board for buffering and level-shifting. The resulting signal (>1 V p-p into 50 Ohms) is routed to the instrument's FREQUENCY STANDARD OUTPUT connector. The 10 MHz signal is also used as a clock for the System Timing Counter (A6U41) located on the A6 DMA/Gate assembly.

7B-25. Output Buffer Stage

As mentioned before, one output of the 500 MHz VCO stage's differential amplifier A14U7 is sent to the divider chain for division by 500. A14U7's other output, pin 5, goes to the "Output Buffer" stage. The 500 MHz signal passes through coupling capacitor A14C21 and into the output buffer. 10 dB amplifiers A14U8 and U10 form an AC-coupled, 50-ohm network. Located at the output of A14U10 is a tuned stub in the form of a 1.5 inch trace on the printed circuit board. This stub provides an ideal open circuit at 500 MHz and a short at frequencies at 1 GHz. This traps unwanted 1 GHz energy while passing a clean 500 MHz sine wave, Components A14R26-C26 and A14R28-C31 form a power splitter and provide DC isolation. The output of the "Output Buffer" stage are two 500 MHz clock signals; CLKA, routed through connector J9 to the A4 assembly, and CLKB, routed through connector J10 to the A5 assembly.

7B-26. A1/A14 Timebase Control/Multiplier Board Troubleshooting

A1 TIMEBASE CONTROL BOARD (HP Part Number 05371-60001)
A14 TIMEBASE MULTIPLIER BOARD (HP Part Number 05371-60014)

EQUIPMENT NEEDED:
- HP 1725A Oscilloscope (or equivalent)
- HP 3325A Function Generator
- HP 54100A Digitizing Oscilloscope
- A16 RF Extender Board, P/N 05371-60016

DIAGNOSTICS:
1) Diagnostic Test 2 – Time Base
2) Diagnostic Test 3 – Input Pods
3) Error 107 – 500 MHz Oscillator Out Of Lock
4) Error 108 – Channel A and B overvoltage
5) Error 109 – Channel A overvoltage
6) Error 110 – Channel B overvoltage

7B-27. BACKGROUND

The A1 Timebase Control and the A14 Timebase Multiplier Assemblies work closely together. The A14 assembly receives a 1 MHz signal from the A1 assembly and multiplies it to 500 MHz. A phase-lock loop circuit keeps the 500 MHz signal locked at 500 MHz and produces a VCO tuning voltage for out-of-lock detection on the A1 assembly. The A1 out-of-lock detection circuit in turn controls the A1 1 MHz signal that is routed to the A14 assembly. Together, these two boards create one large feedback loop. If something fails in this loop, the entire loop becomes is inoperative.

Other functions on the A1 assembly include: 1) the buffering, detection and selection of either 1, 2, 5, or 10 MHz external time base input or the internal ovenized 10811-60111 oscillator, 2) overvoltage detection for both Channel A and B inputs, 3) input pod detection, and 4) the 10 MHz reference output buffer.

Other functions on the A14 assembly include: 1) the generation of the DMA clock (125 MHz) for the A5 ZDT/Count board's RAM-Write circuit, and 2) the generation of the buffered 10 MHz buffered output reference frequency.

	EECL	ECL	TTL
Logic 1	0 v	–0.8 v	5 v
Logic 0	–0.5 v	–1.7 v	0 v

7B-28. A1 AND A14 TROUBLESHOOTING APPROACH

The approach to troubleshooting these two assemblies is to first narrow the failure to one of the two assemblies. Then narrow the failure to a particular circuit on the failed assembly. Then the failure is narrowed down to the component level.

A troubleshooting procedure for each failure symptom (see Failure Symptoms) has been written. Follow the procedure that matches the failure symptom.

7B-29. A1 AND A14 FAILURE SYMPTOMS

The following is a list of failure symptoms that indicate a failure on the A1 assembly only.

1. Error 108 – Channel A and B overvoltage (Not responding properly)
2. Error 109 – Channel A overvoltage (Not responding properly)
3. Error 110 – Channel B overvoltage (Not responding properly)
4. Diagnostic Test 3 – Input Pods Failed

The following is a list of failure symptoms indicating a possible failure on both the A1 or A14 assembly.

1. Error 107 – 500 MHz Oscillator out of lock
2. Diagnostic Test 2 – Time Base Failed

7B-30. A1 AND A14 TROUBLESHOOTING PREPARATION

Remove the top cover of the HP 5371A and place the A1 assembly on its extender board, P/N 05371-60016. Remove the right side cover of the HP 5371A. Then remove the RF cavity cover to expose the A14 assembly. Both assemblies are now ready for troubleshooting.

7B-31. A1 AND A14 TROUBLESHOOTING PROCEDURES

A. ERROR 108, 109 or 110 OVERVOLTAGE MESSAGE NOT WORKING PROPERLY

Indicates failure in A1 Overload Sense Channel A and Channel B circuits.

1. With a no overload signal (below 2.5 Vp-p) at Channel A, A1U7(4) should be at a TTL level high. If not, trace the failure back to the failed component.

2. With an overload signal (greater than 2.5 Vp-p less than 100 kHz, applied momentarily) at Channel A, A1U7(4) should be at a TTL level low. If not, trace the failure back to the failed component.

3. With a no overload signal (below 2.5 Vp-p) at Channel B, A1U7(6) should be at a TTL level high. If not, trace the failure back to the failed component.

4. With an overload signal (greater than 2.5 Vp-p less than 100 kHz, applied momentarily) at Channel B, A1U7(6) should be at a TTL level low. If not, trace the failure back to the failed component.

B. DIAGNOSTIC TEST 3 – INPUT PODS FAILED OR POD ID INCORRECT

Indicates a failure with either the input pod, the A1 Pod ID Latch circuit, or the A1 Input Pod Power Supply circuit.

1. First verify the Input Pod Power Supply circuit is supplying +10 v at A1U26(2) and at A1U14(2) and -10 v at A1U33(2) and at A1U1(2). If any of these voltages are bad, trace the failure to the bad component.

2. Press TEST on the 5371A front panel to enter the Test menu. Run Diagnostic Test 3 – Input Pods. Make certain the Until Fail softkey indicates "Off".

3. Verify the following TTL levels:

A1U29	A1U30
Pin 1 = High	Pin 1 = High
Pin 2 = Low	Pin 2 = High
Pin 3 = Low	Pin 3 = High
Pin 4 = High	Pin 4 = High
Pin 5 = Low	Pin 5 = High
Pin 6 = Low	Pin 6 = Low
Pin 7 = Low	Pin 7 = Low
Pin 8 = High	Pin 9 = Low
Pin 9 = Low	Pin 19 = High
Pin 19 = High	

4. Verify signals A1U29(11-18) and A1U30(11-18) with an oscilloscope. See *Figure 7B-1*.

C. DIAGNOSTIC TEST 2 TIME BASE FAILED OR ERROR 107 – 500 MHz OSCILLATOR OUT OF LOCK MESSAGE OR BOTH

Indicates a failure with either the timebase, the A1 Timebase Detect circuit, or the A1 Reference Output Buffer, or the A14 Timebase Multiplier Assembly.

1. Use an HP 3325A to apply a 1 Vp-p 10 MHz square wave to the rear panel external time base input. Repower-up the HP 5371A. If the time base failure and/or Error 107 message goes away, then go to Part D, A1 Time Base Detect Circuit Troubleshooting. Otherwise continue to STEP 2.

2. Next verify that the VT500, A1U22(5), control voltage is between 1 and +9 Volts. Typically, the VT500 control voltage is at +5 Volts.

3. Verify the presence of a 1 MHz signal at A1U11(4). See *Figure 7B-2*. The signal may not be exactly 1 MHz, but will be approximate. If the 1 MHz signal is present, then go to part B, A14 Time Base Multiplier Troubleshooting. Otherwise, continue to STEP 4.

4. Verify the INTLOCKED signal is a TTL logic level low at A1U7(8). If it is not, then replace A1U22. Otherwise, continue to STEP 5.

5. Verify that the inputs at A1U11(5,6,12) are at ECL logic levels high, low and high, respectively. If they are not, then replace A1U11. Otherwise, continue to STEP 6.

6. Trace the failure from A1U11 back to A1U10 and replace the bad component.

	1 MHz	2 MHz	5 MHz	10 MHz
A1U11(5)	LOW	LOW	LOW	HIGH
A1U11(6)	LOW	LOW	HIGH	LOW
A1U11(12)	LOW	HIGH	LOW	HIGH

A. A1 TIMEBASE DETECT CIRCUIT TROUBLESHOOTING

1. Remove the external time base input from the rear panel of the HP 5371A to enable the internal timebase.

2. Verify that A1DS1, red LED at the top of A1, is lit. (A1DS1 indicates the presence of the internal timebase.) If it is not lit, then trace the failure back to the internal timebase, replacing the failed component. Otherwise, continue to STEP 3.

3. Verify that the +15OSC signal is at +15 volts. This powers the internal timebase. If not, trace the failure back to A1U24A, replacing the bad component. Otherwise, continue to STEP 4.

4. Verify that a 10 MHz signal is present at A1U12(2). If not, trace the failure back to A1U7E (A1U7(10) =TTL High, A1U7(11) =TTL Low). See *Figure 7B-3*.

5. Reapply the 1 Vp-p 10 MHz square wave from the HP 3325A to the HP 5371A rear panel external time base input.

6. Verify that a 10MHz signal is present at A1U12(2). If not, trace the failure back to A1U24, replacing the bad component. (A1U7(10) =TTL High, A1U7(11) =TTL Low.) See *Figure 7B-4*.

B. A14 TIME BASE MULTIPLIER ASSEMBLY TROUBLESHOOTING

1. With an HP 54100A Oscilloscope, verify the presence of an approximate 500 MHz signal at A14U5(9). See *Figure 7B-5*. If signal is present, proceed to STEP 2. If signal is not present, cut one end of A14R32, and apply +5 Volts to A14R27, again check for an approximate 500 MHz at A14U5(9). If no signal, trace the failure back to the A14 500 MHz VCO circuit, replacing the bad component. Be sure to reconnect A14R32 when repairs are made.

2. Verify the presence of a 250 MHz signal at A14U3(15). See *Figure 7B-6*. If not, replace A14U5. Otherwise, continue to STEP 3.

3. Verify the presence of a 50 MHz signal at A14U1(7). See *Figure 7B-7*. If not, replace A14U3. Otherwise, continue to STEP 4.

4. Verify the presence of a 10 MHz signal at A14U4(12). See *Figure 7B-8*. If not, replace A14U1. Otherwise, continue to STEP 5.

5. Verify the presence of a 1 MHz signal at A14U4(2). See *Figure 7B-9*. If not, replace A14U4. Otherwise, continue to STEP 6.

6. Replace A14U6 and A14U9.

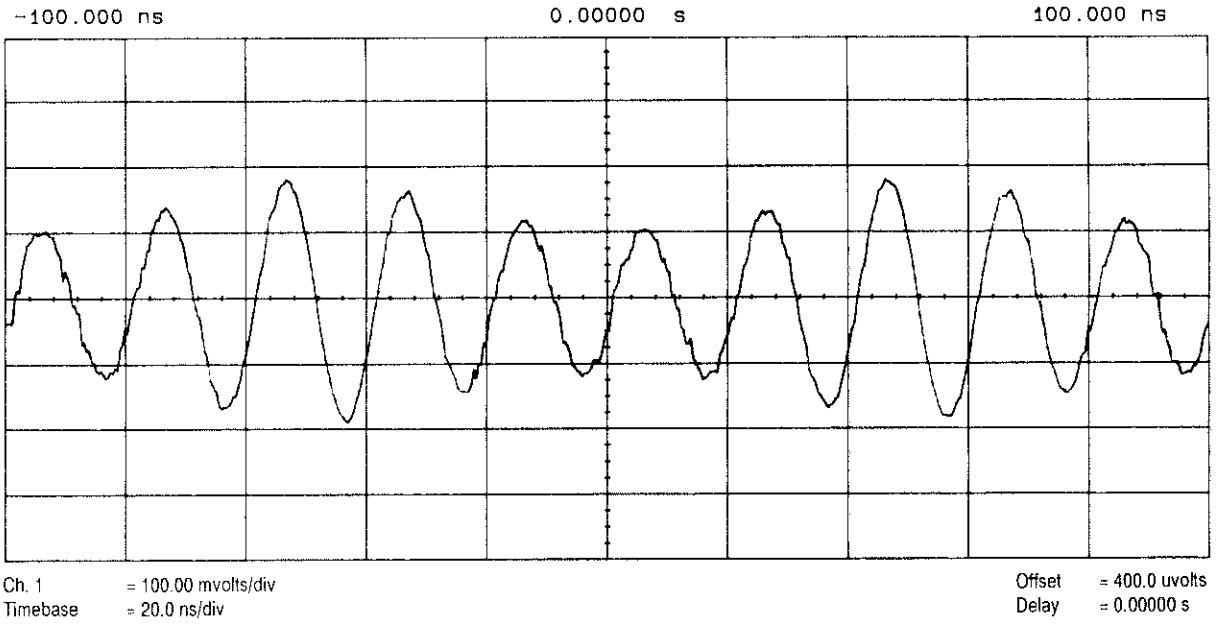


Figure 7B-1. A1U29 (11–18), A1U30 (11–18) Waveform

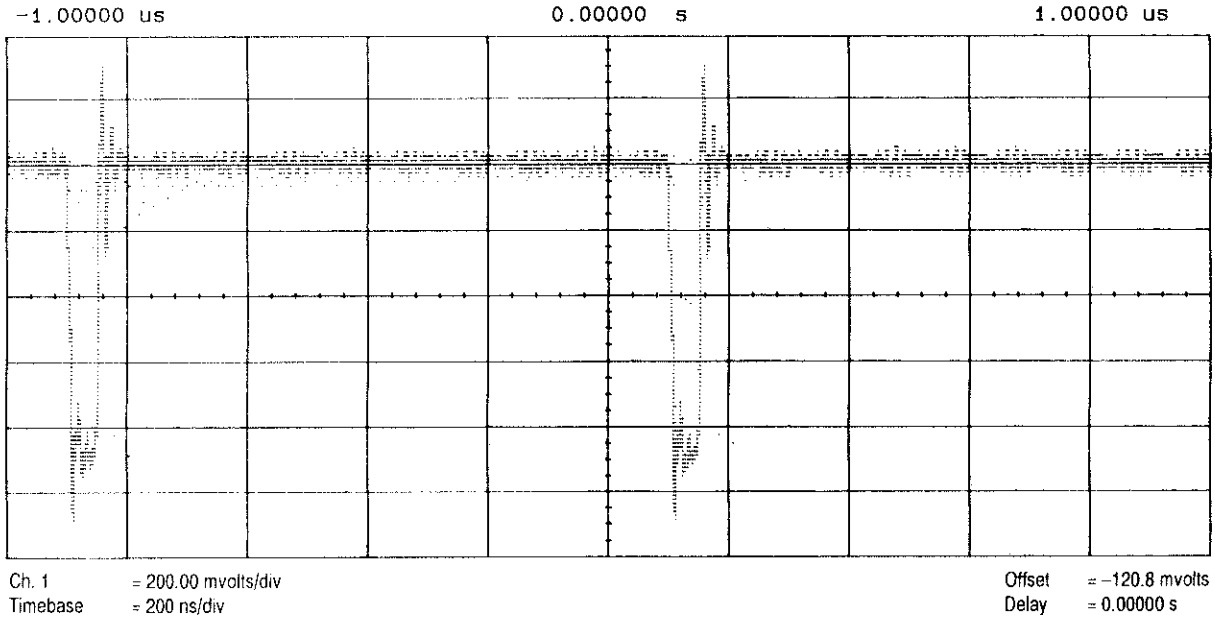


Figure 7B-2. A1U11 (4) Waveform

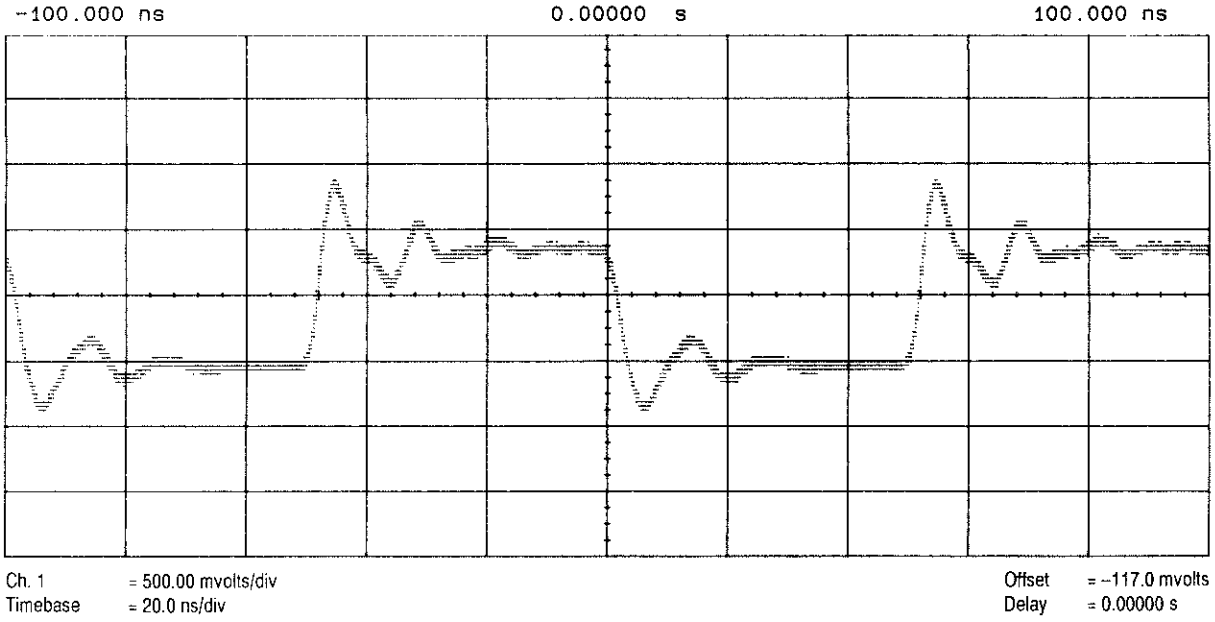


Figure 7B-3. A1U12 (2) Waveform

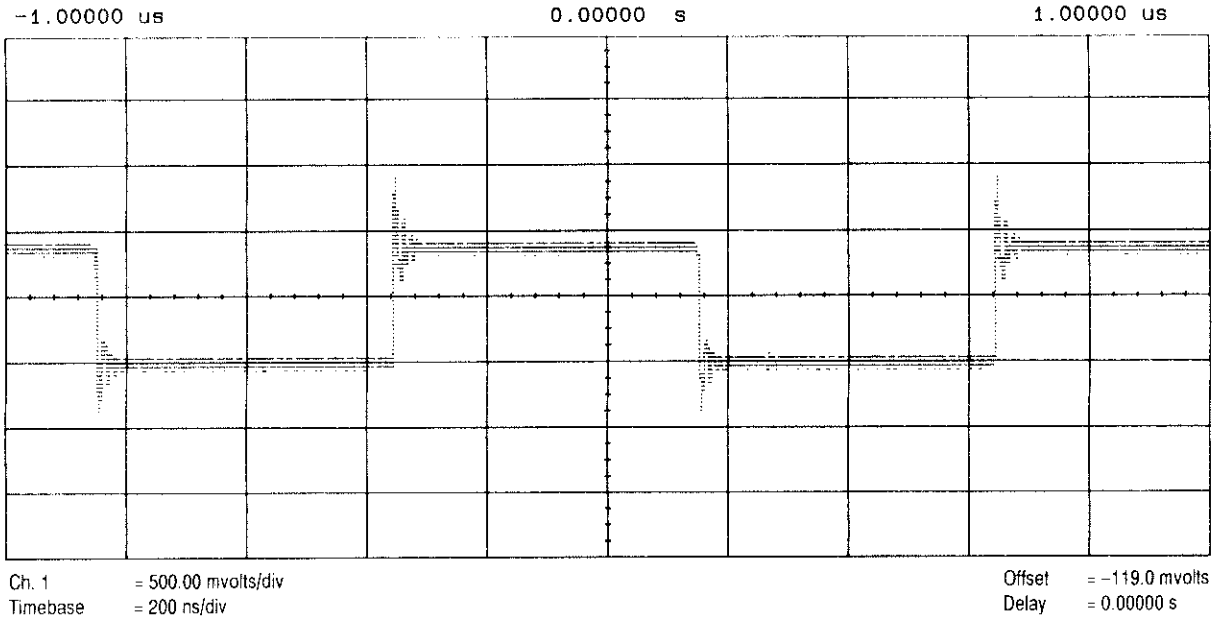


Figure 7B-4. A1U12 (2) Waveform

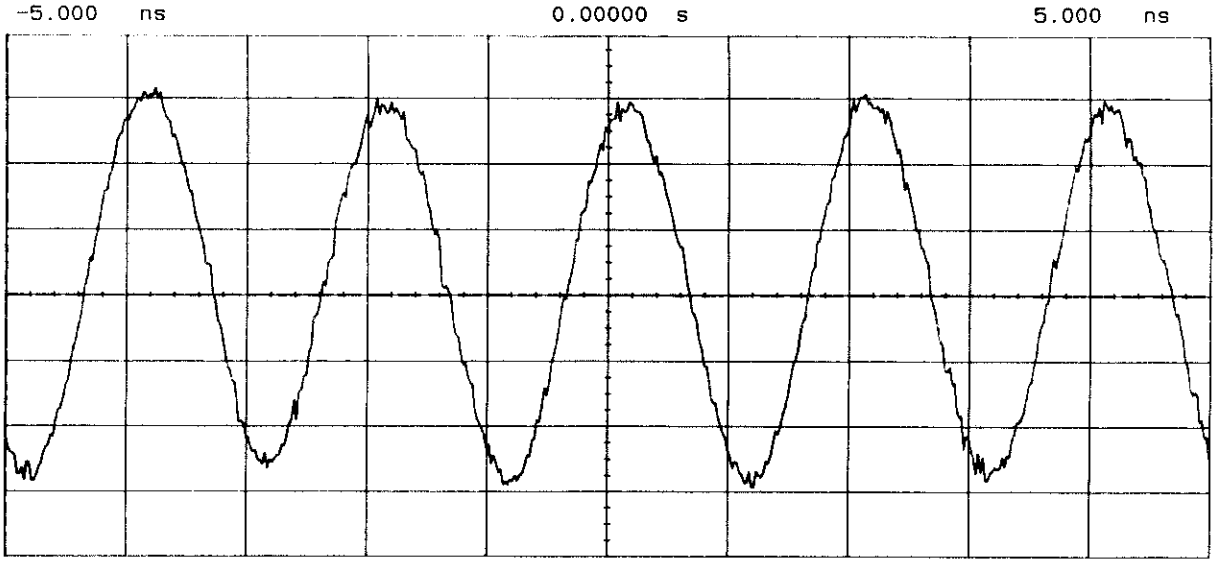


Figure 7B-5. A14U5 (9) Waveform

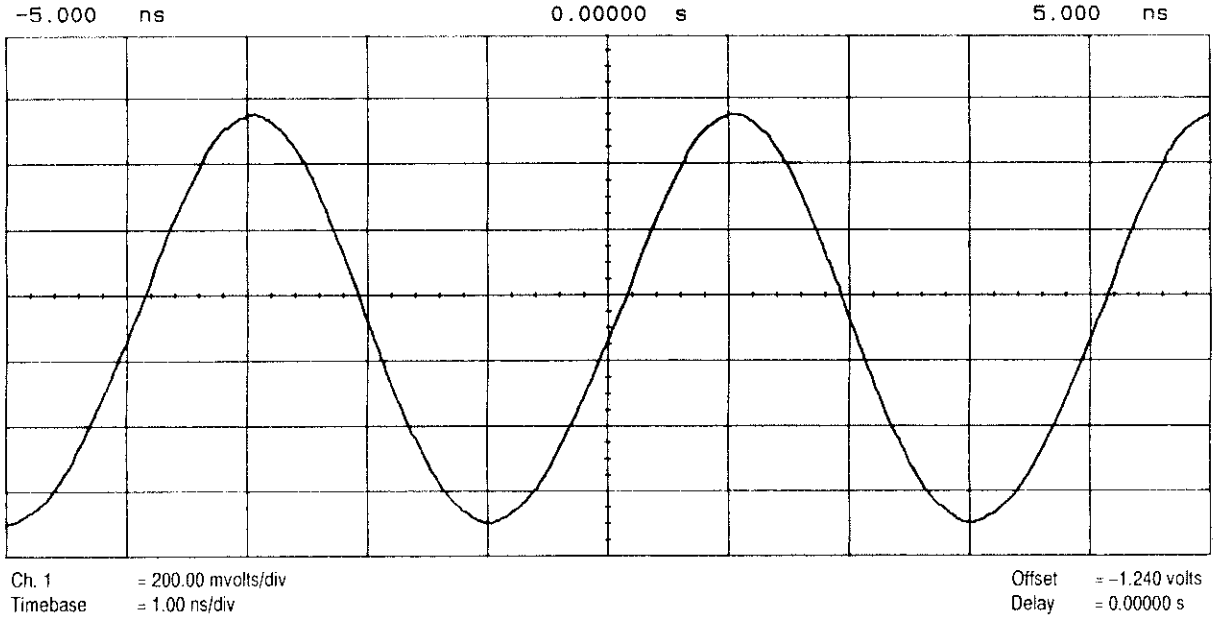


Figure 7B-6. A14U3 (15) Waveform

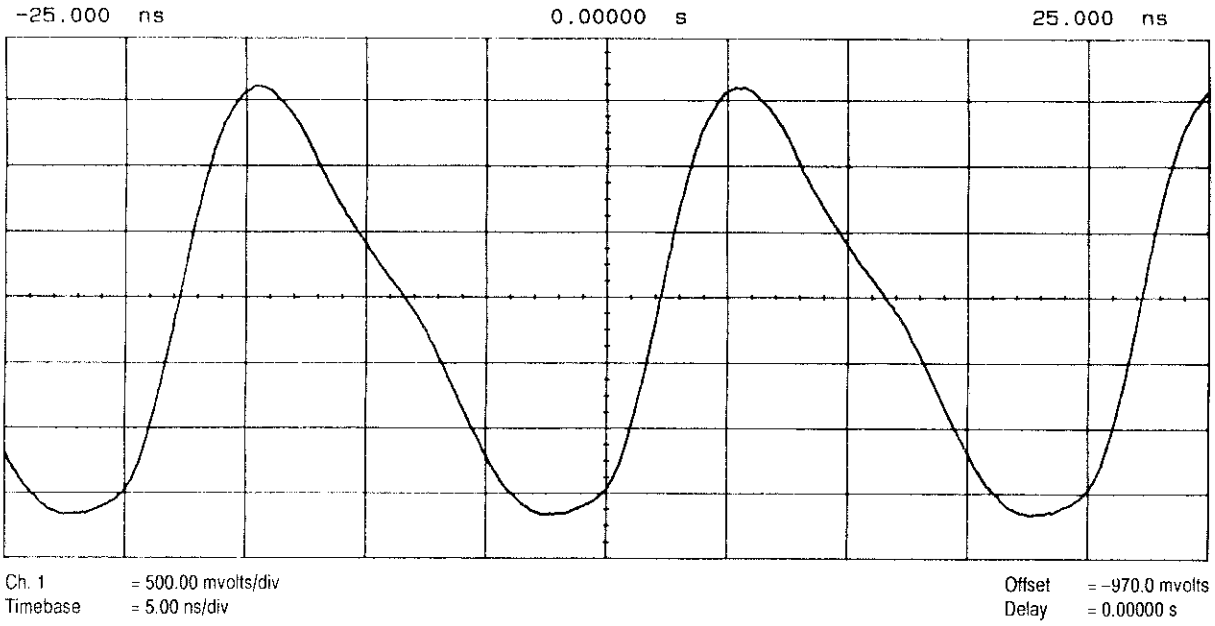


Figure 7B-7. A14U1 (7) Waveform

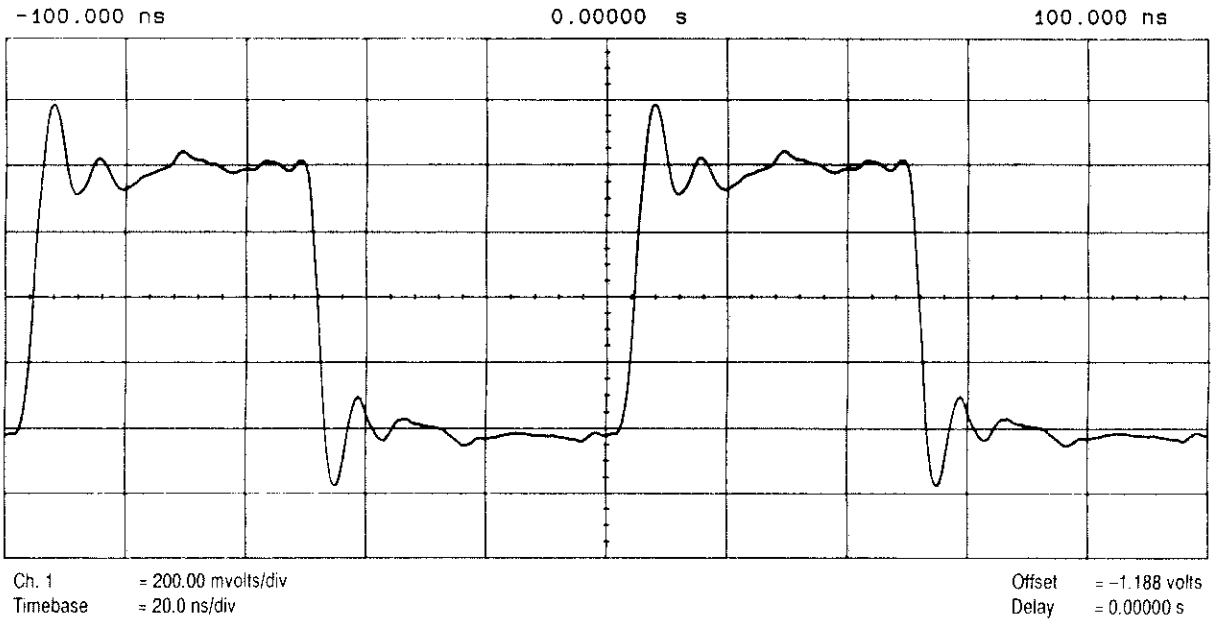


Figure 7B-8. A14U4 (12) Waveform

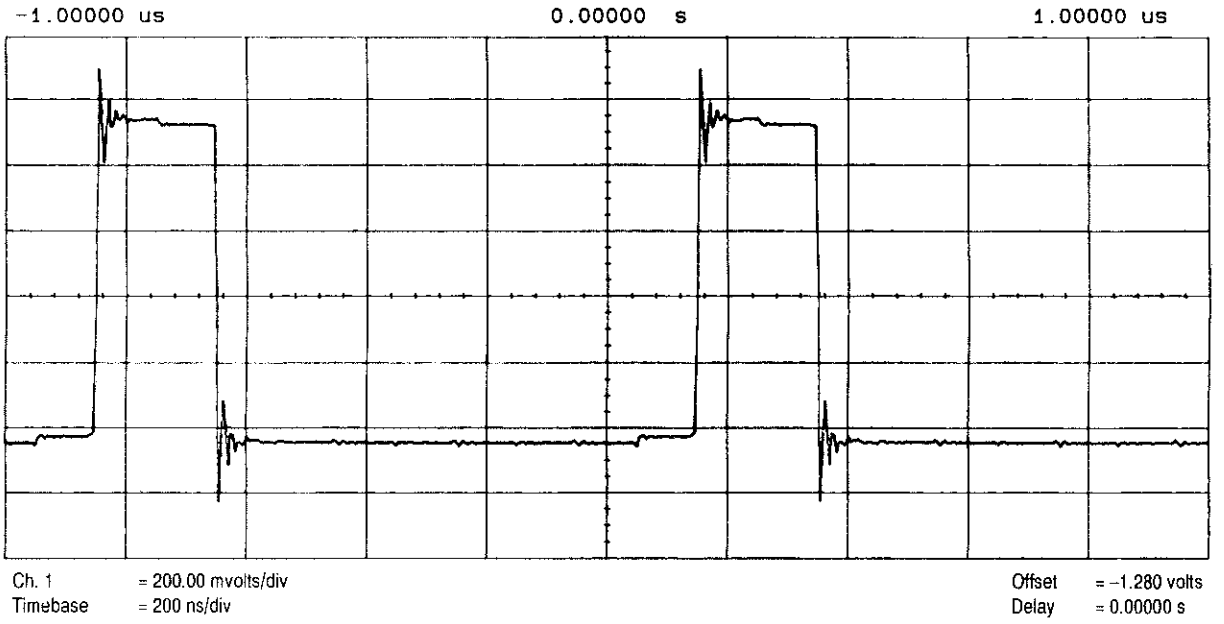
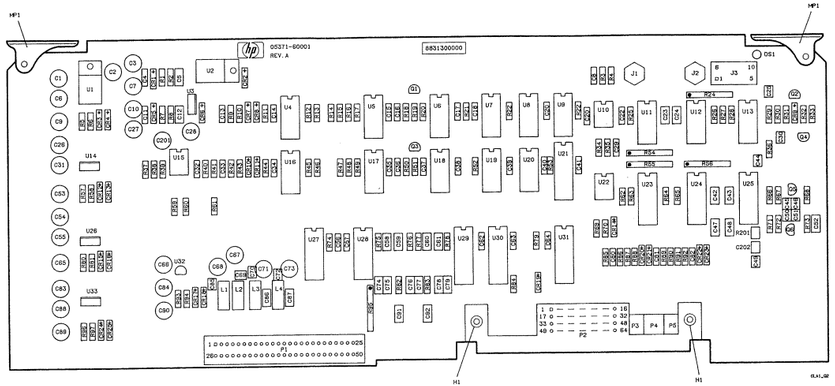


Figure 7B-9. A14U4 (2) Waveform



A1 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A1 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THE "C CHANNEL POWER SUPPLY" IS NOT USED IN THE "A" VERSION OF THE 5371. THESE PARTS MAY NOT BE LOADED.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

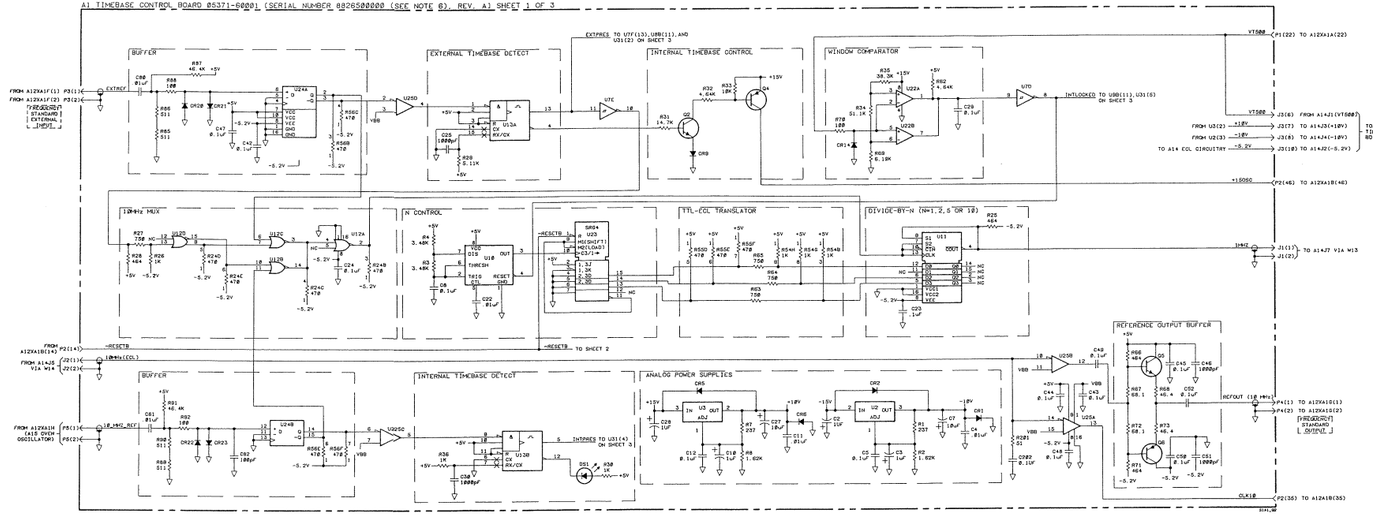
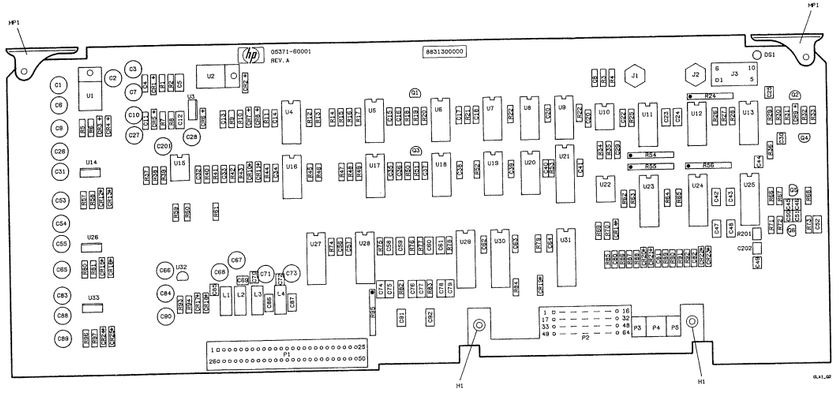


Figure 7B-10. A1 Time Base Control Board, Schematic Diagram (Sheet 1 of 3)



A1 SCHEMATIC DIAGRAM NOTES

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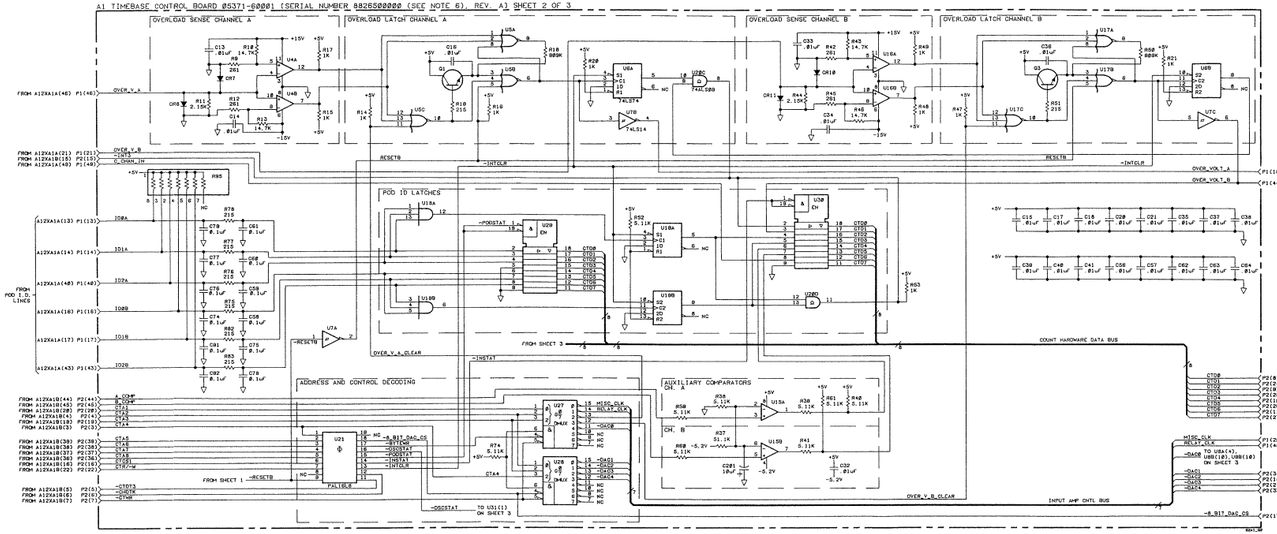
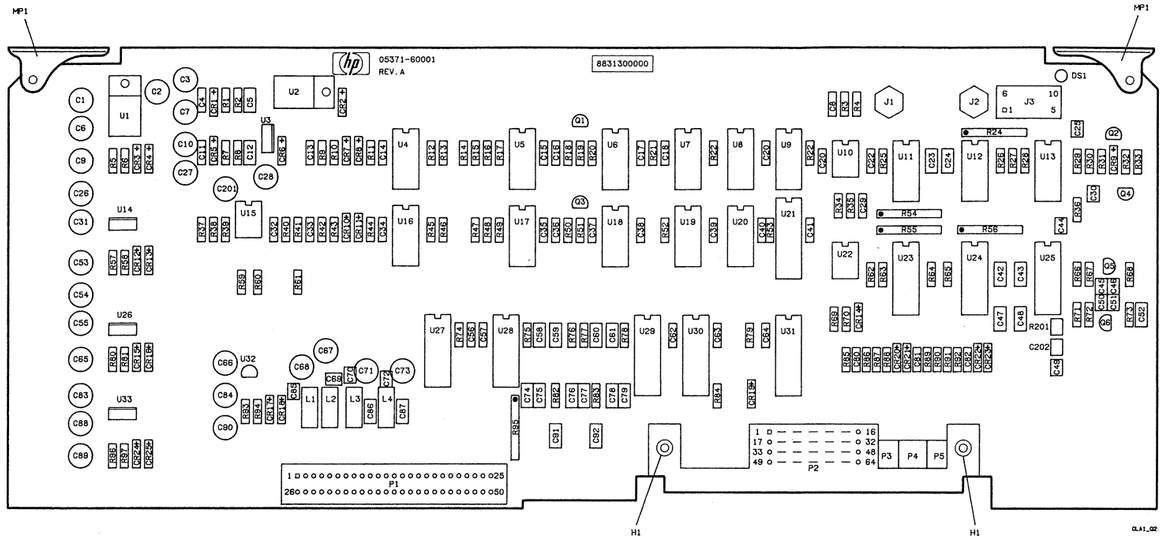


Figure 7B-10. A1 Time Base Control Board, Schematic Diagram (Sheet 2 of 3)



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   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THE "C CHANNEL POWER SUPPLY" IS NOT USED IN THE "A" VERSION OF THE 5371. THESE PARTS MAY NOT BE LOADED.
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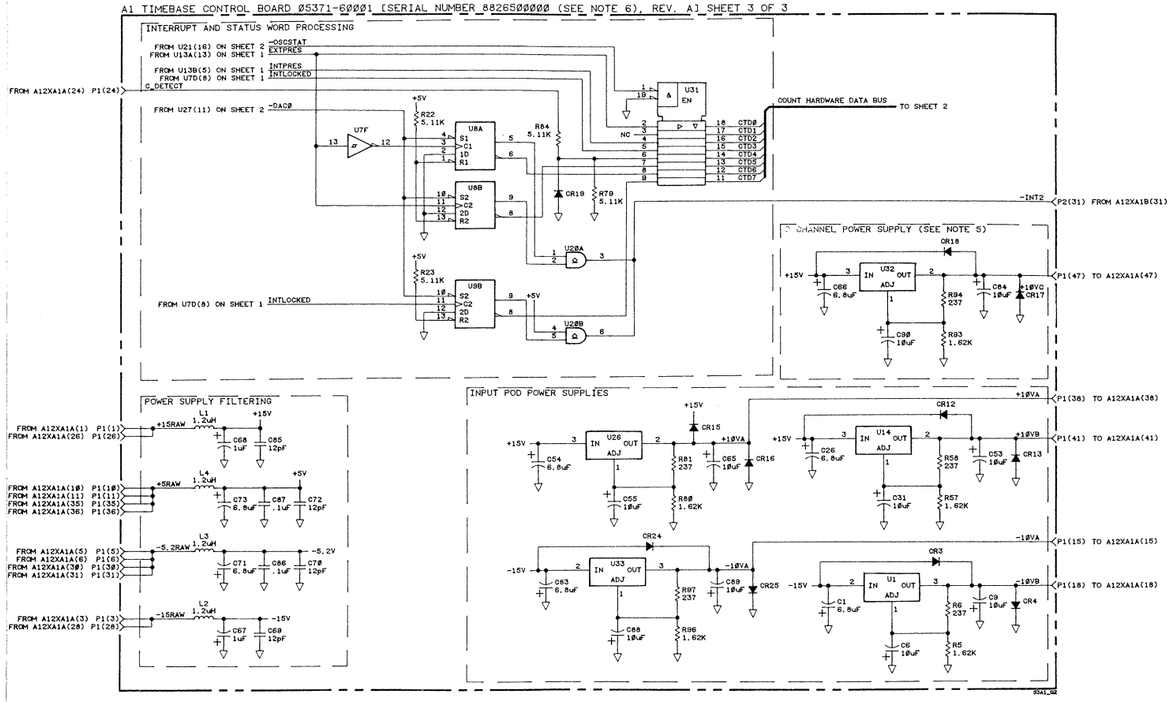
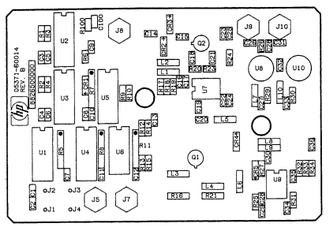


Figure 7B-10. A1 Time Base Control Board, Schematic Diagram (Sheet 3 of 3)



A14 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A14 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THESE COMPONENTS ARE CONSTRUCTED FROM THE PC BOARD MATERIAL ITSELF.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

A14 TIMEBASE MULTIPLIER BOARD 05371-60014 (SERIAL NUMBER 3820S00000 (SEE NOTE 6), REV. B)

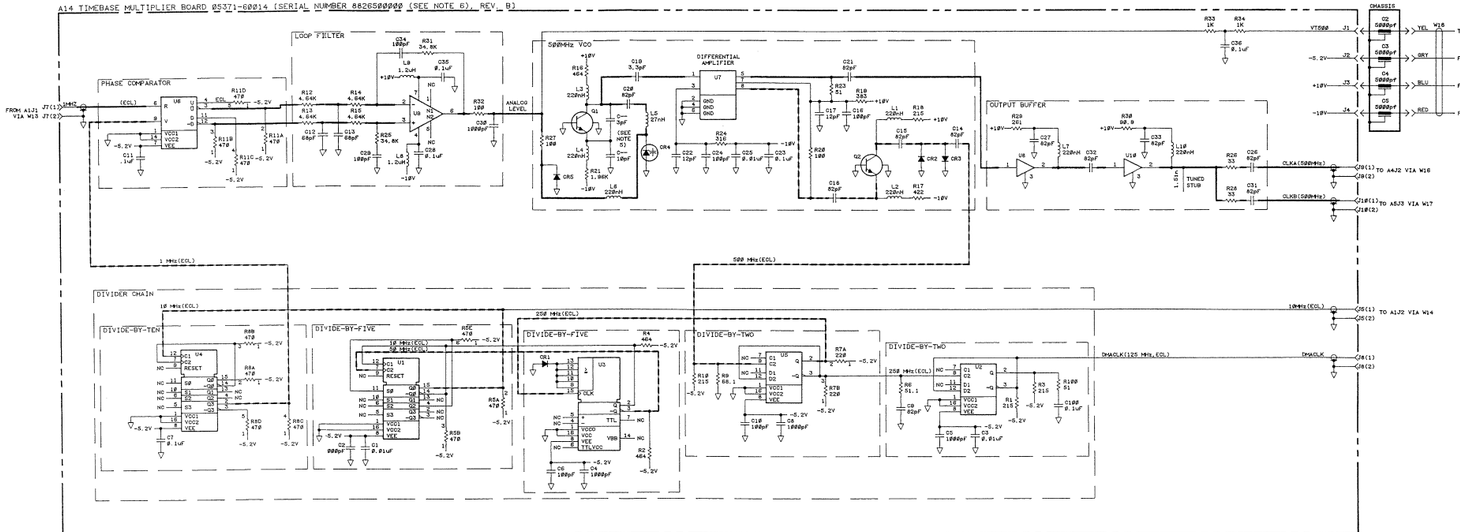


Figure 7B-11. A14 Timebase Multiplier, Schematic Diagram

SECTION 7C
A2 INPUT AMPLIFIER BOARD

7C-1. Introduction

The A2 Input Amplifier Board contains two similar DC coupled 500 MHz amplifier circuits, CHANNEL A and CHANNEL B. Both circuits accept input signals from either the front-panel 50Ω Input Pods or the rear-panel Option 060 connector inputs without any loss of input sensitivity or change in input impedance. The input signals are conditioned and translated to EECL logic level square waves (0V logic "high", –800 mV logic "low") and routed through coaxial cables to the A5 ZDT/Count Board's counting circuitry. The A2 assembly hardware can be configured from either the HP 5371A front panel INPUT menu screen or via the HP-IB interface. All data transfer occurs over the Count Hardware Data Bus (CTD0-CTD11).

Signal conditioning is controlled by relay switches A2K1 through A2K4. These relays set X2.5 or X1 attenuation, COMMON A or SEPARATE signal paths, 0 or -2V termination bias voltage, and provide over-voltage protection for the input circuitry. The relays are driven by a TTL driver, which is programmed by the A7 Processor Board's 68000 microprocessor via the Count Hardware Data Bus lines (CTD0-CTD7). The signal conditioning parameters are set according to the front panel CRT setup or HP-IB commands.

In summary, the functions performed by A2 Input Amplifier Board are as follows:

- Provides hardware control of signal pathways when either the COMMON or SEPARATE input channel modes are selected,
- Controls the trigger slope and trigger level voltage setting,
- Provides 50Ω signal path termination,
- Allows selection of either 0-volt (TTL logic) or –2-volt (ECL logic) termination bias voltage,
- Provides over-voltage protection for the HP 5371A, and
- Detects presence of an input signal at either of the front panel CHANNEL A or B input connectors,
- Measures ± Vp used for Peak Measurements and for setting the automatic trigger level (Single and Repetitive modes).

The two identical A2 amplifiers are fully programmable and designed to optimize pulse fidelity. The following theory describes only CHANNEL A, since the CHANNEL B circuit is similar. See the "A2 Input Amplifier Board Block Diagram" in *Figure 7C-9* for reference.

7C-2. Channel Input Mode

CHANNEL A is the primary input channel for the HP 5371A. All counter measurement functions can be performed on a signal directed to this channel. CHANNEL B is an alternate input channel with input characteristics matching those of CHANNEL A. To use each channel separately, the SEPARATE input mode is selected via the INPUT menu. The signal from CHANNEL A can also be simultaneously applied to CHANNEL B by selecting the COMMON input mode. When COMMON input mode is selected, relays A2K1, K2, K4, and K8 route the input signal at CHANNEL A to both CHANNEL A and B's input and counting circuitry. Simultaneously, relay A2K8 disconnects CHANNEL B input signal from CHANNEL B input and counting circuitry and is routed by relay A2K7 to CHANNEL A's *Termination* and *Termination Bias* circuitry. This ensures proper loading of both user signal source inputs. The counter's input impedance and signal sensitivity do not change when input modes are changed from SEPARATE to COMMON and vice versa. This process maintains waveform fidelity and the counter's frequency response.

7C-3. Termination Bias Voltage

With the 50Ω HP 54002A Input Pod installed, either CHANNEL A, B, or A & B, may be programmed to route the input signal through the diode-clamped DC Offset IC input pin 2 (pin 4 for CHANNEL B), through a 50Ω resistor (A2R42), and into 0 or –2 Volts of termination bias voltage. The –2-volt bias voltage preserves the fidelity of high-speed ECL signals and eliminates the need for external probing when measuring ECL circuits. The 8 dB attenuator (A2U1) cannot be programmed when ECL attenuation has been selected since ECL input signals are already low in amplitude. –2 Volt ECL termination is programmable only with the 50Ω Pod (HP 54002A) installed. The HP 54001A [1 GHz Miniature Active Probe (10:1, 10 kilohm) and HP 54003A (1 Megohm Probe)] are isolated by high impedance from the A2 Input Amplifier Board. When either the HP 54001A or HP 54003A input pods are installed, the 0 Volt termination voltage is programmed automatically.

7C-4. CHANNEL A Input Description

7C-5. CHANNEL A INPUT

The HP 54002A 50Ω input pod is electrically a dead short. The input signal terminates into 50Ω resistance(A2R42) ONLY after the HP 5371A is powered on. After passing through the input pod, the signal routes through coaxial cable W24, joins cable W19 at the forward chassis bulkhead, and continues on through cable W19 to connector A2J1. The input signal then travels in one of two directions. If the 1:1 (0 dB) attenuation setting is selected, relays A2K1 and K2 short CHANNEL A attenuator A2U1 out of the circuit. In the 2.5:1 (8 dB) attenuation setting, A2U1 is placed in series with the CHANNEL A input signal. This setting allows the application of an input signal with a peak voltage of 2.5 times the normal operating range. Immediately following relay A2K2, the input signal is sampled and routed to the A1 Timebase Control Board's *Overload Sense* circuit via signal path OVER V A. This circuit protects the A2 Input Amplifier by opening relays A2K1 and K2 when the input voltage exceeds the nominal value of ±2.7 Volts. See *Path Selection (Relay Control)* circuit description for more details.

7C-6. DC OFFSET (CHANNEL A)

The CHANNEL A input signal continues to CHANNEL A DC Offset IC A2U2, pin 2. A2U2 is simply a buffer amplifier, having an operating range of 0 to 500 MHz, that allows application of a programmable ± 2 VDC offset to the input signal. (Refer to *Figure 7C-1.*) At pin 2 (pin 4 for CHANNEL B), the input signal is diode-clamped to ±5 Volts for over-current protection. The input signal exits A2U2 through pin 4 (pin 2 for CHANNEL B) for off-chip termination through 50Ω resistor (A2R42) and into 0V or –2V termination bias voltage of the *Termination Bias* circuitry. The DC levels of the input and output signals are sampled by the A2U2's external feedback loop comprised of comparator A2U6. The INPUT SENSE DC level, A2U2 (pin 1), and the OUTPUT SENSE DC level, A2U2 (pin 13), are compared by A2U6. The output error voltage of A2U6, pin 6, returns to the *DC Offset* stage of the DC Offset IC where it sets the programmed DC output level. This external feedback loop is adjustable for unity gain over A2U2's usable bandwidth using potentiometer A2R4, the CHA DC Offset Adjust. When this loop is properly adjusted, the low frequency response matches the high frequency response. Consequently, no error voltage is introduced by lower frequency input signals. This error voltage is also routed through connector A2P1 (pin 49) to Test Connector A12J6 and used for in-factory test purposes. Diodes A2CR5 and CR6 prevent the latch-up of the external feedback loop.

Adjustable resistor A2R3, CH A Input Bias Loop Adjust, allows for elimination of offsets caused by internal resistances of the DC Offset IC. This adjustment is made by imputing a 10 Hz signal and adjusting A2R3 until the control voltage measured at pin 17 of A2U2 is minimized.

Transistor A2Q2, Zener diode A2CR2, and associated resistors provide the DC Offset IC A2U2 (pin 16) with +8 Volts power. Transistor A2Q1, Zener A2CR1, and its associated resistors provide A2U2 (pin 10) with –10 Volt power.

The programmable trigger level is applied to the CHANNEL A input signal at pin 14 of DC Offset IC, A2U2. The analog trigger level voltage is generated by a 12-bit digital-to-analog converter (DAC), A2U20, which is programmable in discrete steps over the input range of the instrument. The DAC interfaces directly with the CTD0-CTD11 bits of the Count Hardware Data Bus. The DAC is enabled by toggling its Chip Select (~CS) pin low with signal DAC 4 generated by the A1 Timebase Control Board. Before the DC offset voltage is applied to the DC Offset IC, the DAC's output passes through an inverting buffer amplifier A2U19. Adjustment potentiometer A2R14, CHA Input Amp Gain Adjust, allows compensation of the circuit for any offsets introduced by the circuit components. (See *Trigger Level Control* paragraphs for a more detailed description of how the HP 5371A sets input trigger level and performs peak amplitude measurements.)

Pin 12 of the DC Offset IC, A2U2, is the signal output port of the IC. This signal has an amplitude equal to the input signal at pin 2 minus the programmed offset at pin 14. From here, the input signal connects directly to input pin 3 of CHANNEL A's Comparator IC, A2U4.

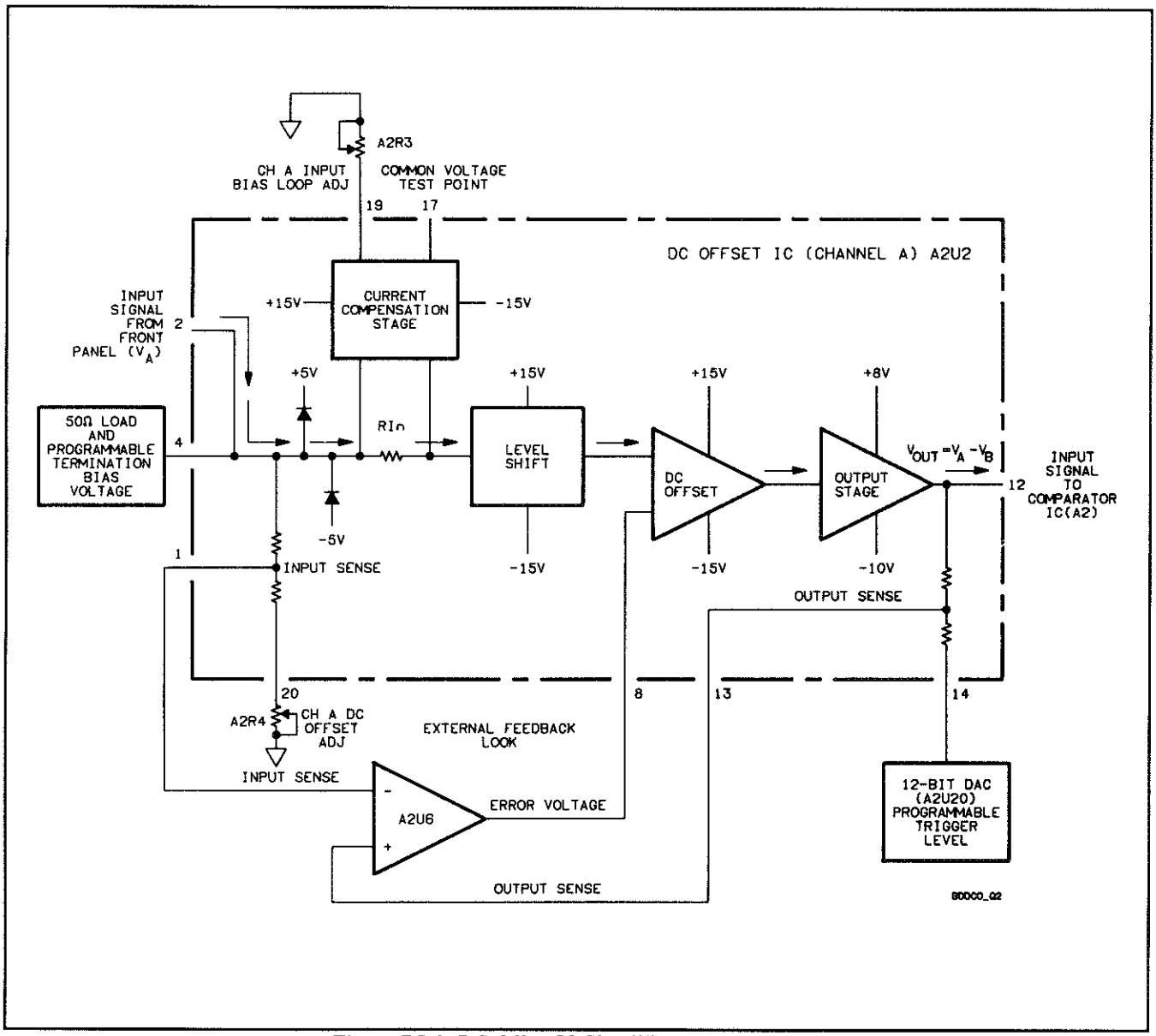


Figure 7C-1. DC Offset IC Simplified Block Diagram

7C-7. COMPARATOR IC

Comparator IC A2U4 converts the single-ended signal from the DC Offset IC, A2U2, to a differential EECL-level, digital output signal for use by the A5 ZDT/Count Board's counting hardware. (Refer to *Figure 7C-2.*) Respectively, the comparator's *Impedance Switching Bridge* and *Input Diode Bridge* stages terminate the input signal into 50 Ohms and protect the IC from over-voltage conditions. The input amplifier stage converts the single-ended input to a differential output. The signal is then applied to a *Schmitt Trigger* stage which incorporates hysteresis and slope control. The differential, open-collector outputs at pins 13 and 14 are EECL-level digital outputs with amplitudes of 0 Volts (logic "high") or –800 (logic "low") millivolts when terminated into 50 Ohms. The signals at pins 13 and 14 are 180 degrees out of phase with respect to one another. Pin 13 provides the A5 assembly with CHANNEL A count data and Pin 14 output drives the CHANNEL A trigger LED control circuitry.

The Comparator IC permits adjustment of total system offset (A2R10) and upper and lower hysteresis limits (A2R12), and control of trigger slope selection.

- CHANNEL A Total System Offset Adjust (A2R10) — This adjustment establishes the trigger level at zero (0) Volts on a low distortion sine wave. This adjustment is made with a CHANNEL A input of 1 kHz at 30 mV p-p sine wave and the CHANNEL A DAC (A2U20) set at mid-range (i.e., 0 Volts). The output amplitude of comparator A2U4, as measured between resistor A2R24 and connector A2P2 (pin 44), is set at its minimum level by adjusting A2R10.

- CHANNEL A Hysteresis Adjust (A2R12) — This adjustment is made with a CHANNEL A input of 100 Hz at 100 mV p-p sine wave and the CHANNEL A DAC (A2U20) set at mid-range (i.e., 0 Volts). The hysteresis is then adjusted so that the hysteresis window difference between the upper hysteresis point and lower hysteresis point, is 8 mV p-p (or 0 ± 4 mV).

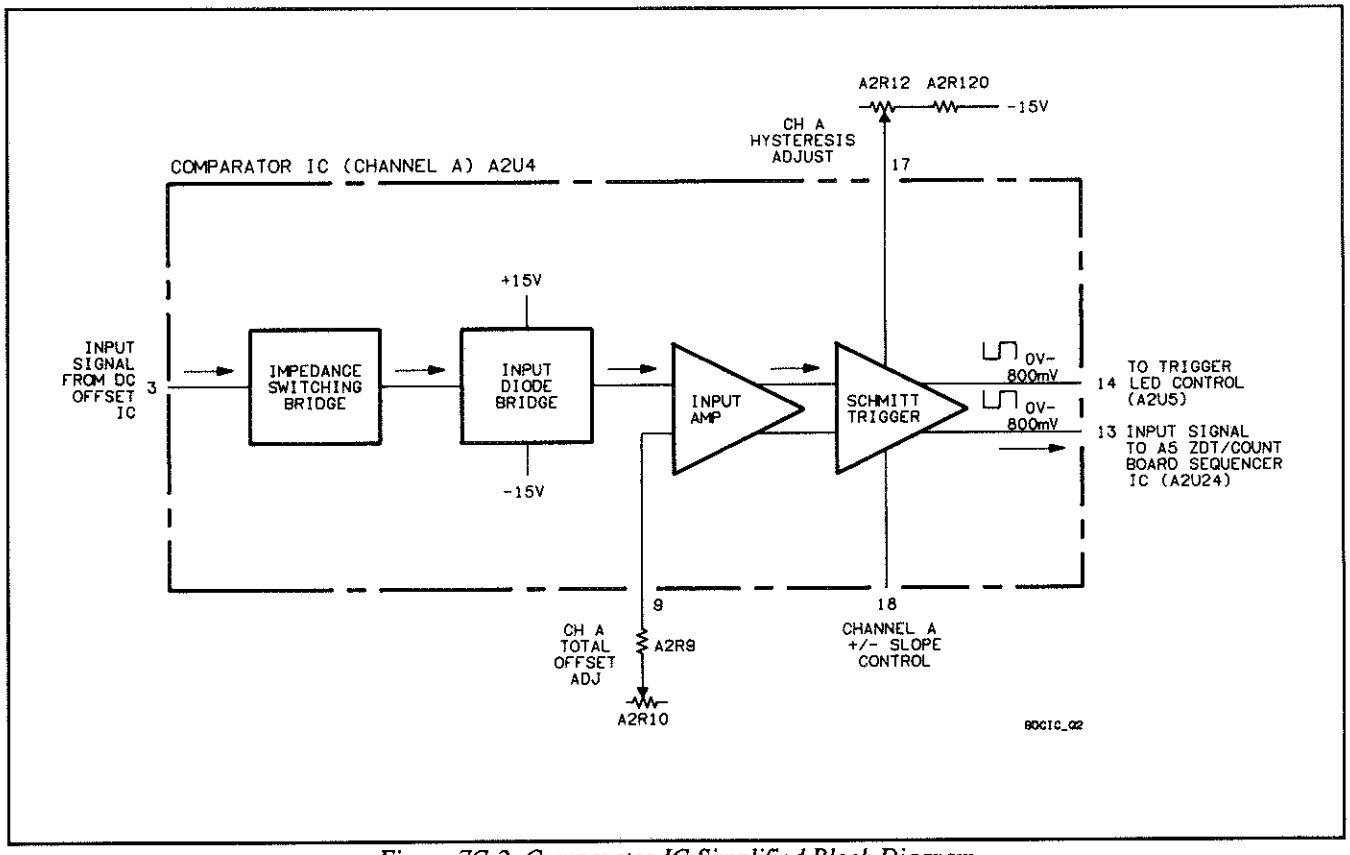


Figure 7C-2. Comparator IC Simplified Block Diagram

- Channel A Slope Control — Slope control determines whether the A2U4 Comparator IC triggers an output at the upper hysteresis limit (+4 mV) on the input signal's positive-going edge, or at the lower hysteresis limit (–4 mV) on the input signal's negative-going edge. Slope control is programmed by the A7 Processor Board's 68000 microprocessor in the form of TTL level 0- or +4-volt bit. Flip-flop A2U16, pin 16, is set at 0 Volts for a positive trigger slope, and +4 Volts for a negative trigger slope. This TTL signal is applied to the *Schmitt Comparator* stage of A2U4 via pin 18.

7C-8. TRIGGER LEVEL CONTROL AND PEAK AMPLITUDE MEASUREMENT

The trigger level control circuit varies the DC content of the input signal until the positive and negative edges pass through the upper and lower hysteresis limits (+4 mV and –4 mV respectively) of Comparator IC, A2U4. The hysteresis limits are the voltage levels required by the Comparator IC to trigger and change its output state. Selection of positive slope triggering forces the Comparator IC to trigger at its upper hysteresis limit while selection of negative slope triggering forces triggering at its lower hysteresis limit. Once the Comparator IC has triggered, it cannot retrigger until the input signal crosses the opposite hysteresis limit. In the case of the Comparator IC, the signal must pass through a hysteresis window of 8 mV p-p centered at zero Volts. (Refer to *Figure 7C-3.*)

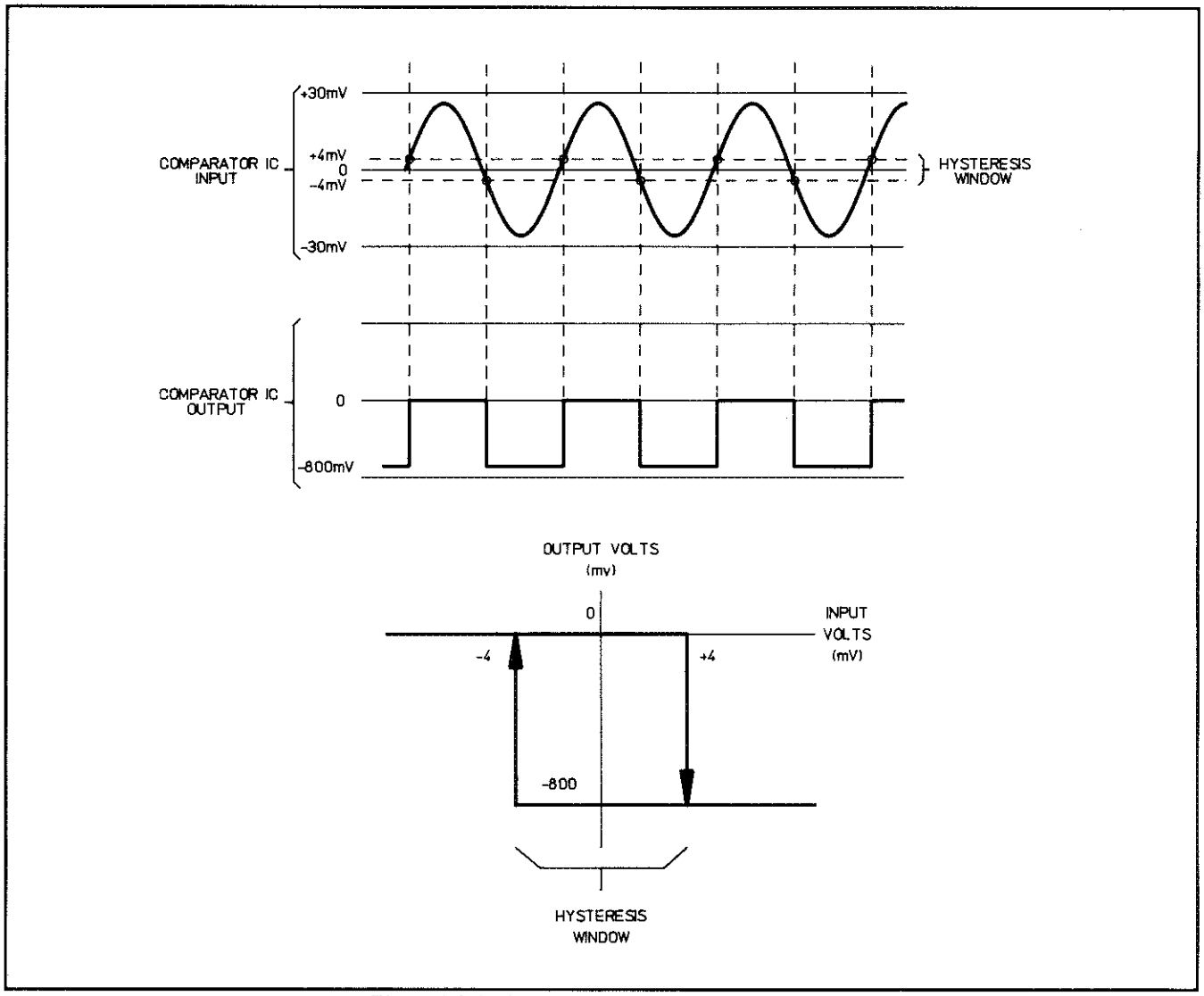


Figure 7C-3. Comparator IC Hysteresis Window

The method used for setting the input trigger level depends on which HP 5371A trigger mode is selected: Manual or Automatic. In the Manual Trigger mode, the numeric value of the DC offset is manually entered (with 2 mV resolution) through the front-panel DATA ENTRY keypad or ENTRY/MARKER control knob. The A7 Processor Board's 68000 microprocessor reads the data entered and sends a 12-bit digital offset equivalent to A2 assembly's Digital-to-Analog Converter (DAC), A2U20. The DAC's output is buffered and applied to pin 14 of the DC Offset IC, A2U14, where it adds to or subtracts from the DC content of the input signal. The programmed offset and choice of trigger slope specifies at which hysteresis limit the Comparator IC will trigger. The front-panel CHANNEL A trigger LED will flash at a 10 Hz rate when the DC offset is adjusted correctly. The flashing trigger LED indicates that the input signal passes through the upper and lower hysteresis limits (+4 mV and –4 mV).

Two Automatic Trigger level setting modes can be selected: Single or Repetitive. In both Single and Repetitive Automatic Trigger modes, the maximum and minimum signal amplitudes are measured and then the Automatic trigger level voltage is set by selecting a percentage (0% to 100%) of the measured peak-to-peak amplitude. The trigger level percentage is user-selected, in 1% increments, via the front-panel DATA ENTRY keypad or ENTRY/MARKER control knob. When set in SINGLE AUTO TRIGger mode, the trigger level voltage is set automatically either at the beginning of the first measurement block, whenever SINGLE AUTO TRIGger mode is selected, after the front-panel RESTART key is pressed, or at any time a measurement restarts as a result of making a parameter change via the FUNCTION or INPUT menu screens. The trigger level voltage is maintained for subsequent measurement blocks. But when REPETITIVE AUTO TRIGger mode is used, the trigger level voltage is set at the beginning of each measurement block or whenever REPETITIVE AUTO TRIGger mode is selected.

The Automatic Trigger level voltage is set as follows. (Refer to *Figure 7C-4*.) Assume that an AC signal within the dynamic operating range of the HP 5371A and having sufficient positive DC offset so that the Comparator IC will not trigger is applied to the front-panel CHANNEL A BNC connector. The Comparator IC output is monitored by the A1 Timebase Control Board's *CHA Auxiliary Comparator* stage via the ~A COMP signal line. The output of the auxiliary comparator is latched onto the Count Hardware Data Bus (bits CTD0-CTD7) by the A1 *Pod ID Latches* stage. The A7 Processor Board's 68000 microprocessor (A7U8) reads and interprets this bit, and responds with an incremental change in offset value. This modified offset data returns to the A2 assembly's DAC, A2U20, via the Count Hardware Data Bus (bits CTD0-CTD11). This DC offset output level is buffered and inverted by amplifier A2U19 and applied to the DC Offset IC at pin 14. Monitoring of the Comparator IC output and the incremental change of the DC offset continues until the input signal's AC component passes through the upper and lower hysteresis limits, triggering the Comparator IC. The DC offset is again modified until the positive peak of the input signal falls just below the upper hysteresis limit of +4 mV. At this point, the Comparator IC will again stop triggering. The 68000 microprocessor records the total amount of DC offset applied so far. The polarity of the DC offset is now reversed and applied in increments until the Comparator IC begins to trigger again. The DC offset continues to change until the input signal's negative peak no longer crosses the lower hysteresis limit of –4 mV. Again, the Comparator IC stops triggering. The 68000 microprocessor uses the ± DC offsets to calculate the +Vp, –Vp, and Vp-p of the CHANNEL A input signal. Vp-p is multiplied by the user-selected percentage trigger point. A DC offset that shifts the input signal so that the selected trigger percentage point of V p-p coincides with the upper hysteresis limit (+4 mV) of the IC Comparator IC is now applied.

If after a measurement period of 5 seconds (default value) an input signal is not detected, a momentary message, "Waiting for signal...", is displayed on the HP 5371A CRT Status Line.

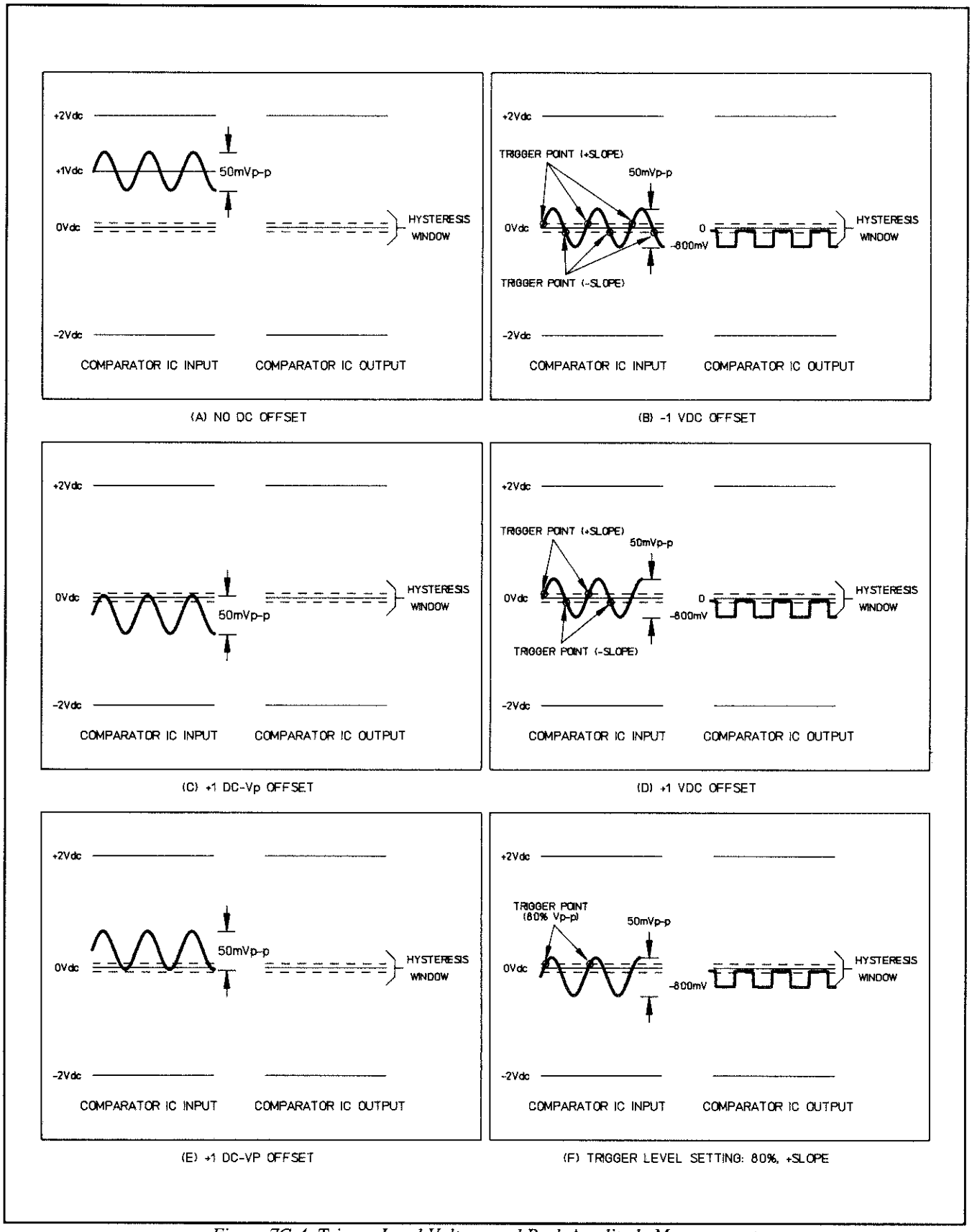


Figure 7C-4. Trigger Level Voltage and Peak Amplitude Measurement

7C-9. TRIGGER LED CONTROL

Output pin 14 of Comparator IC A2U4 is terminated into 50 Ohms (A2R35) and routed to flip-flop A2U5, which is designed specifically for high speed EECL signals. This flip-flop, along with a printed circuit board delay line, stretches the pulse to between 1 and 2 nanoseconds. The signal then enters a one-shot multivibrator comprised of transistors A2Q3 and Q6, producing a 400 nanosecond negative-going pulse. This 400 nanosecond is again stretched to 100 milliseconds (10 Hz) by transistors A2Q4 and Q5. The output signal, which is tapped off the collector of A2Q5, routs through NAND gate A2U12A, and drives the front-panel CHANNEL A trigger LED (A11DS8). The CHANNEL A trigger LED provides the user with a visual indication that adequate CHANNEL A input signal is present to trigger a measurement. The LED flashes at a 10 Hz rate when CHANNEL A is triggering, but remains off when the input signal is above or below the desired trigger level setting.

7C-10. PATH SELECTION (RELAY CONTROL)

Relays A2K1 through K7 have 50Ω characteristic impedance and low crosstalk characteristics. All relays are controlled by the A7's 68000 microprocessor via Count Hardware Data Bus lines CTD0 through CTD7. The instructions for both Channel's A and B are decoded by flip-flop A7U27. The relays are set by clocking A2U27 with the RELAY CLK signal generated by the A1 Timebase Control Board. The eight A2U27 outputs are sent to relay driver A2U26, which supplies the TTL level voltages required to open and close the relays. A2U27 control bits for relays A2K3, K4, K7, and K8 are routed directly to relay driver A2U26. On the other hand, the A2U27 control bits for CHANNEL A and CHANNEL B relays, A2K1-K2 and A2K5-K6 respectively, are first ANDED with the over-voltage signals generated by the A1 Timebase Control Board circuitry before going to relay driver A2U26. Control bits for relays A2K1 and K2 are ANDed with OVER V A and control bits for relays A2K5 and K6 are ANDed with OVER V B. A TTL logic "low" signal on either OVER V A or OVER V B disables the appropriate CHANNEL A and B relays, providing protection against over-voltage conditions. A hardware interrupt is also generated by the A1 Timebase Control and A2 Input Amplifier circuitry. Over-voltage sense lines A and B are routed from CHANNEL A and B inputs respectively to the *Overload Sense* circuitry located on the A1 Timebase Control Board. If a voltage level greater than approximately ±2.7 Volts is detected at the front-panel input connector, the A1 circuits notify the Hardware Over-ride circuits (A2U28) located on the A2 Input Amplifier Board, which open the appropriate relay disconnecting the over-voltage condition from the HP 5371A. After the relays open, which occurs within milliseconds of the over-voltage detection, an error message is displayed on the CRT display. It is left to the user to correct the over-voltage condition and reset the HP 5371A. An example of an error message displayed for an over-voltage condition on CHANNEL A would be "Error 109: Ch A Overvoltage".

7C-11. TERMINATION BIAS, ±SLOPE, TRIGGER LED

Flip-flop A2U16 latches the Termination Bias, ±Slope, and Trigger LED control bits from the Count Hardware Data Bus. Data is clocked from the bus by the positive-going edge of the TTL-level MISC CLK signal generated by the A1 Timebase Control Board. The function of these control bits are as follows:

- Data bits CTD0 and CTD1 provide a two-bit binary address to four-channel multiplexer A2U7.
- Data bits CTD2 and CTD3 provide a two-bit binary address to four-channel multiplexer A2U21.
- Data bit CTD4 provides independent enabling of CHANNEL B's front-panel trigger LED.
- Data bit CTD5 provides independent enabling of CHANNEL A's front-panel trigger LED.
- Data bit CTD6 provides slope control to the CHANNEL A Comparator IC, A2U4. A TTL low (0 Volts) instructs the Comparator IC to generate an output pulse on the positive-going edge of the input signal, while a TTL high (+4 Volts) instructs it to generate an output pulse on the negative-going edge of the input signal.
- Data bit CTD7 provides slope control to the CHANNEL B Comparator IC, A2U14. A TTL low (0 Volts) instructs the Comparator IC to generate an output pulse on the positive-going edge of the input signal, while a TTL high (+4 Volts) instructs it to generate an output pulse on the negative-going edge of the input signal.

7C-12. TERMINATION BIAS SELECTION

The main function of A2U7 and U21 multiplexers is the programming of the input channel termination bias voltage to either zero Volts or an ECL level of –2 Volts. A2U7 and op-amp A2U8 set the bias of input CHANNEL A while A2U21 and op-amp A2U22 set the bias of input CHANNEL B. Another function of the multiplexers is to facilitate troubleshooting of CHANNEL A and B hardware. The bias level of both channels can be set at + 1 V p-p for troubleshooting purposes. The relays can be programmed to use CHANNEL A multiplexer A2U7 in CHANNEL B and Channel B's multiplexer A2U21 in CHANNEL A.

Multiplexers A2U7 and U21 provide programmable paths for four inputs (pins 4, 5, 6, and 7) to a common output (pin 8) as programmed by address lines A0 and A1 (pins 1 and 16 respectively). A2U7 output (pin 8) goes to the non-inverting input (pin 3) of op-amp A2U8, which sets the DC bias to transistors A2Q7 and Q8 such that their emitter circuits are at 0, –2, or +1 V p-p. Multiplexer A2U21 behaves in a similar fashion.

As mentioned earlier, each multiplexer has four inputs and each input can be selected by a two-bit address specified by the A7 68000 microprocessor. The four possible inputs for the CHANNEL A multiplexer A2U7 are (1) Ground (pin 4), (2) –2 VDC (pin 5), (3) VREF OUT (pin 6) from CHANNEL A DAC A2U20 pin 6, and (4) Channel B DC Offset as set by CHANNEL B DAC A2U30 pin 9. The four possible inputs for the CHANNEL B multiplexer A2U21 are (1) Ground (pin 4), (2) –2 VDC (pin 5), (3) VREF OUT (pin 6) from CHANNEL A DAC A2U20 (pin 6), and (4) CHANNEL A DC Offset as set by CHANNEL A DAC A2U20 pin 9.

7C-13. A2 Input Amplifier Troubleshooting

7C-14. TEST EQUIPMENT REQUIRED

- HP 54100A Digitizing Oscilloscope [with 50Ω Input Pods (HP 54002A)]
- BNC-to-SMC Cable (HP Part Number 05371-60229)
- 50Ω 1:1 Probe (HP Part Number 10437A)
- A19 RF Extender Board (HP 05371-60016)

NOTE

The following procedure applies to both Channel A and Channel B. For Channel B, the relevant ICs and pins are placed within brackets.

7C-15. DIAGNOSTICS

Diagnostic Test 4. Input Amplifier Test

This test checks the following A2 circuit functions:

- Comparators will trigger when an input signal within specs is applied to front panel CHANNEL A or B input,
- Comparators will not trigger when input signals are removed from front panel CHANNEL A or B input,
- Comparators will trigger on either the positive or negative slope of the front panel CHANNEL A or B input,

- Relays K1-K8 are tested in various combinations to ensure functionality, and
- Termination Bias Selection Multiplexers for both CHANNEL A and B are programmed and a peak search is performed on the resulting level.

NOTE

Refer to Section 7E for a more detailed description of Test 4.

To run Test 4, perform the following steps:

A. Turn 5371A front-panel STBY-ON power switch to ON. Wait 4-5 seconds to allow unit self testing to finish.

B. Press 5371A TEST menu selection key. The TEST menu screen is displayed.

C. Move menu cursor to the test desired or enter the test number in the "Test Number" field using the DATA ENTRY numeric keys.

D. Press the RUN softkey to start the test. The Diagnostic Test screen is displayed. The test will run continually until the Stop softkey is pressed, or until another menu key is selected.

E. The test can temporarily halted by pressing the Pause softkey. This suspends the test and freezes any messages on the front-panel CRT display. To resume the test, press Run softkey.

F. The test can also be executed in "Until Fail" mode. The selected test will run continually until a failure occurs. At that time the test enters "pause" mode. Press the "Until Fail" softkey to turn on this function.

7C-16. BACKGROUND

The A2 Input Amplifier Board conditions and converts the CHANNEL A and B input signal into an EECL-level square wave of the same frequency. This square wave is supplied to the A5 ZDT/Count board.

7C-17. A2 INPUT AMPLIFIER TROUBLESHOOTING APPROACH

To check the overall functionality of the A2 assembly, the EECL-level square wave for CHANNELs A and B are verified. The board trouble can be isolated into three major areas; (1) the DC Offset Circuit, (2) the comparator circuit, and (3) Trigger Level Control circuit.

7C-18. A2 TROUBLESHOOTING PROCEDURE

A. Set front panel STBY-ON power switch to STBY.

B. Install A2 assembly in the A19 RF Extender Board, HP Part Number 05371-60016. See Section 7F for installation details.

C. Connect the 5371A rear-panel 10 MHZ OUTPUT signal to 5371A front-panel CHANNEL A input.

D. Press the PRESET button.

E. Set the input triggering mode to MANUAL. Vary the triggering voltage –480 mV to +480 mV. Verify that A2J2 [A2J4] outputs an EECL 10 MHz square wave throughout the whole range of triggering voltage. (See *Figure 7C-5.*)

F. If the signals displayed at output connectors A2J2 [A2J4] are as expected, the A2 assembly is functioning properly. If signals are not as expected, proceed with these procedures.

G. Select SINGLE AUTO trigger. The trigger level voltage should be approximately 0 Volts.

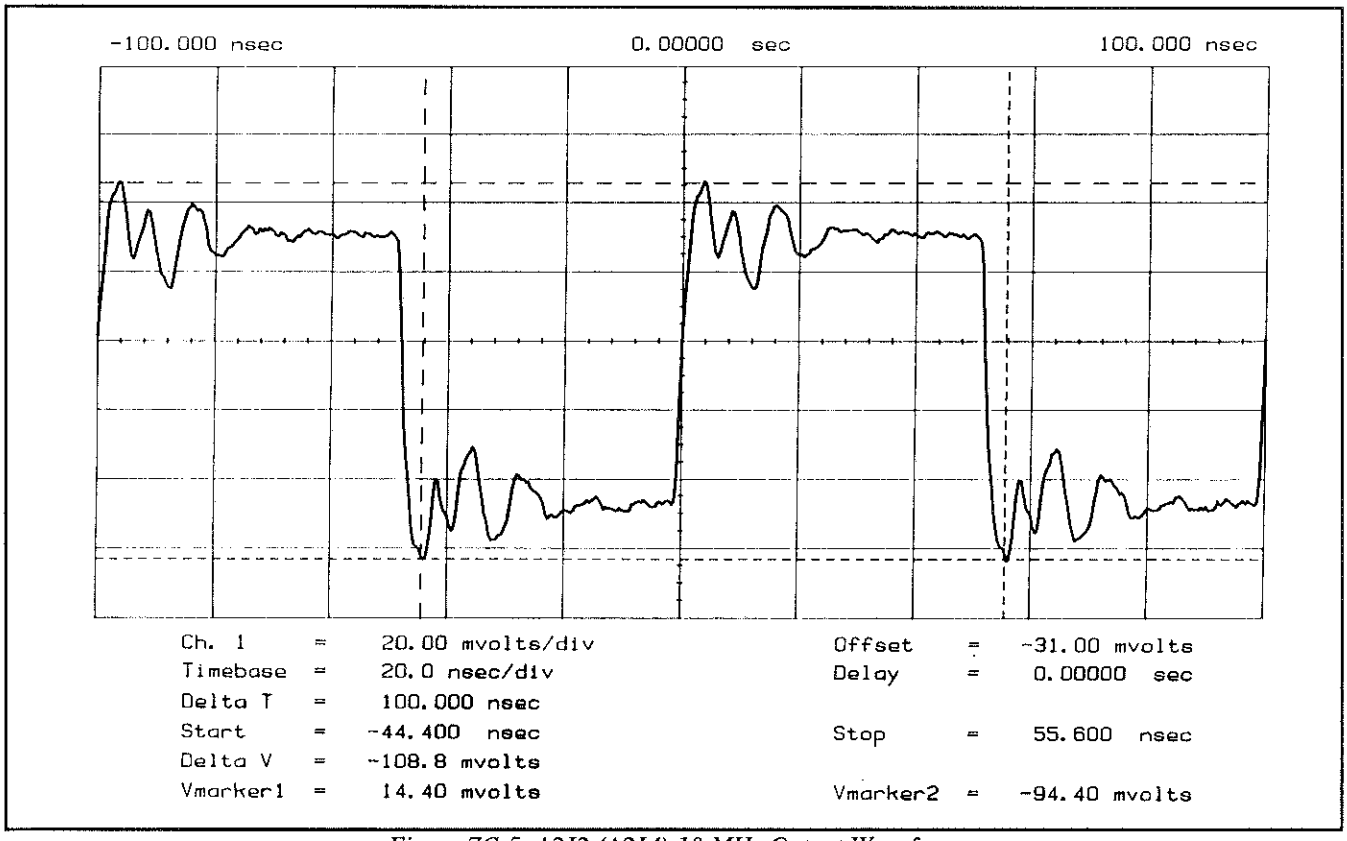


Figure 7C-5. A2J2 (A2J4) 10 MHz Output Waveform

7C-19. DC Offset Hybrid Check

A2U2 [A2U14] is the DC Offset Hybrid that offsets the input signal by a dc voltage equal to the programmed trigger level voltage.

A. Measure the signal at input connector A2J1 [A2J3]. This is the signal applied directly from the input pod and is used as reference for further measurements. The signal is 1 V(p-p).

B. Set trigger level voltage to +480 mV.

C. Pins A2U2(2) and A2U14(2) are the input pins to Channel A and B DC Offset Hybrids respectively. Verify that a TTL-level 10 MHz square wave is at each input (see *Figure 7C-6*). If A2U2(2) [A2U14(4)] appears to be different, check the input paths from input connector A2J1 [A2J3]. If the input path is OK, check and replace the relays A2K1, K2, K3, and K4 [A2K5,K6,K7, and K8]. [Diagnostic Test 4 will check the operation of all relays.

D. Verify that A2U2(14) and A2U14(14) are set at +480 mV. (See *Figure 7C-7.*) If A2U2(14) [A2U14(14)] are not both set at +480 mV, proceed to the "Trigger Level Control Check".

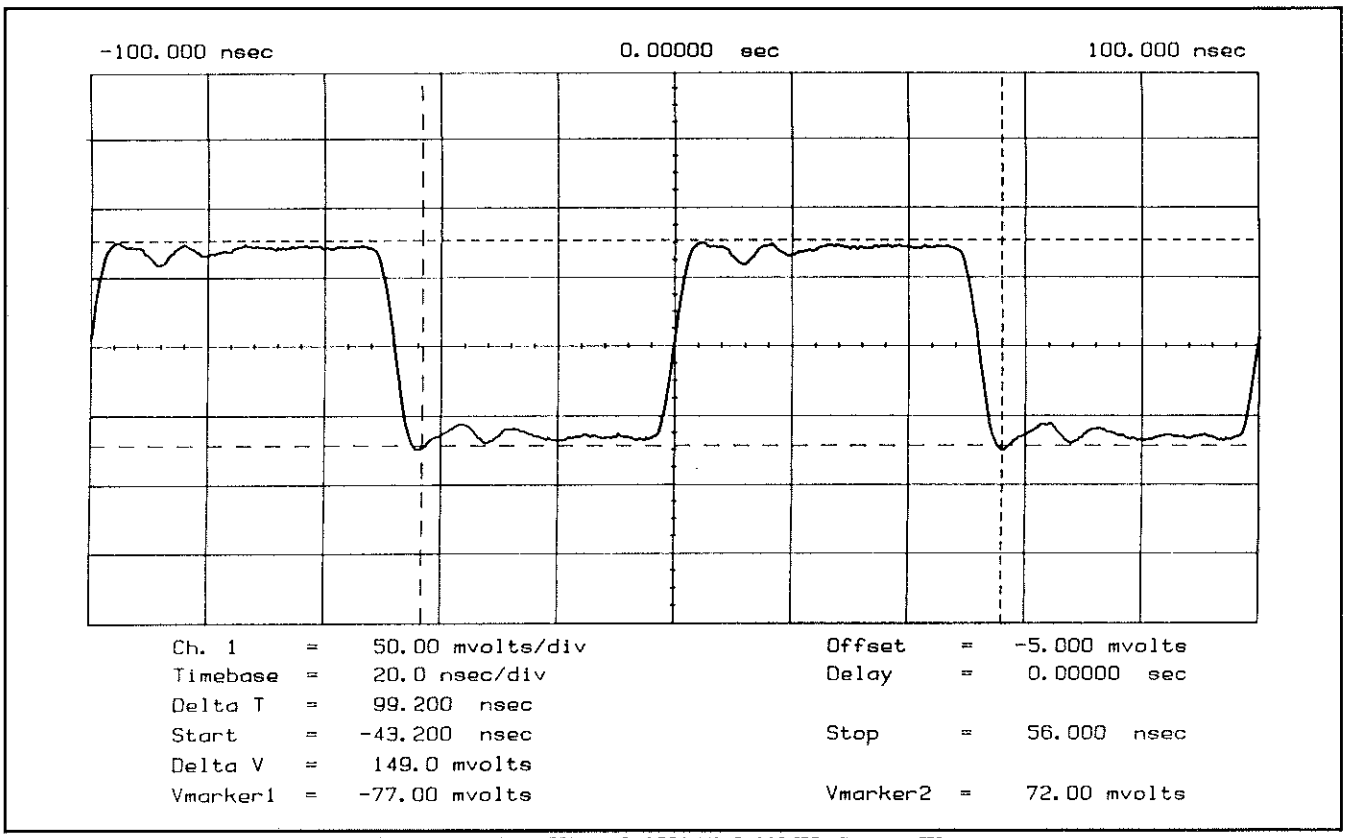


Figure 7C-6. A2U2(2) [A2U14(2)] 10MHz Square Wave

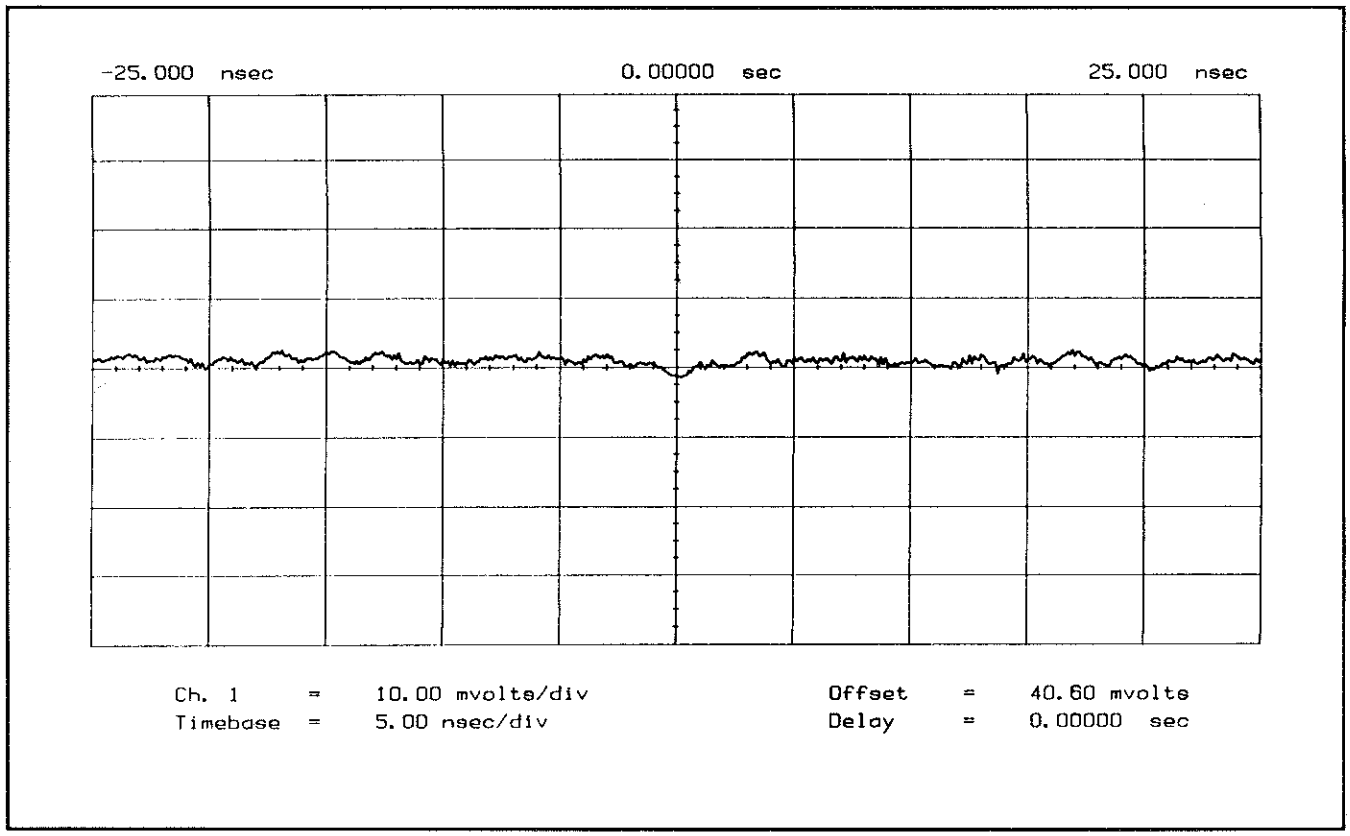


Figure 7C-7. A2U2(14) [A2U14(14) +480 mVolt Setting

E. Press 5371A front panel MANUAL key.

F. Observe DC Offset Hybrid output pin A2U2(12) [A2U14(12)]. In MANUAL trigger mode, vary the trigger level and observe the signal as it dc level shift.

G. If both signals are not correct, replace A2U2 [A2U14].

H. Nominal signal levels of the DC Offset Hybrids, A2U2 [A2U14], are listed in *Table 7C-1*.

Table 7C-1. DC Offset Hybrid Pin Voltages

Pins	Signal
1	400 mV (p-p) (triangle wave)
2	Input Signal
3	–5.2V dc
4	Input Signal
5	+5V dc
6	–15V dc
7	GND
8	–5.2V dc
9	GND
10	–10V dc
11	GND
12	Output Signal
13	400 mV (p-p) (triangle wave)
14	Nominal 20 mV (p-p) (square wave)
15	GND
16	+8V dc
17	–2.5V dc
18	+15V dc
19	0V (Adjustable)
20	0V (Adjustable)

7C-20. Comparator Hybrid Check

The Comparator Hybrid IC, A2U4 [A2U15], which behaves like a Schmitt trigger, outputs a digital EECL square wave whenever the input crosses the ICs hysteresis points of 0 ±4 mV. The Comparators output is sent via a coaxial cable to the A5 ZDT/Count Board for counting.

A. Set triggering level voltage to +480 mV.

B. Measure Comparator input pin A2U4(3) [A2U15(3)]. Ensure that a 10 MHz square wave having a DC offset of –480 mV is measured (see *Figure 7C-8*).

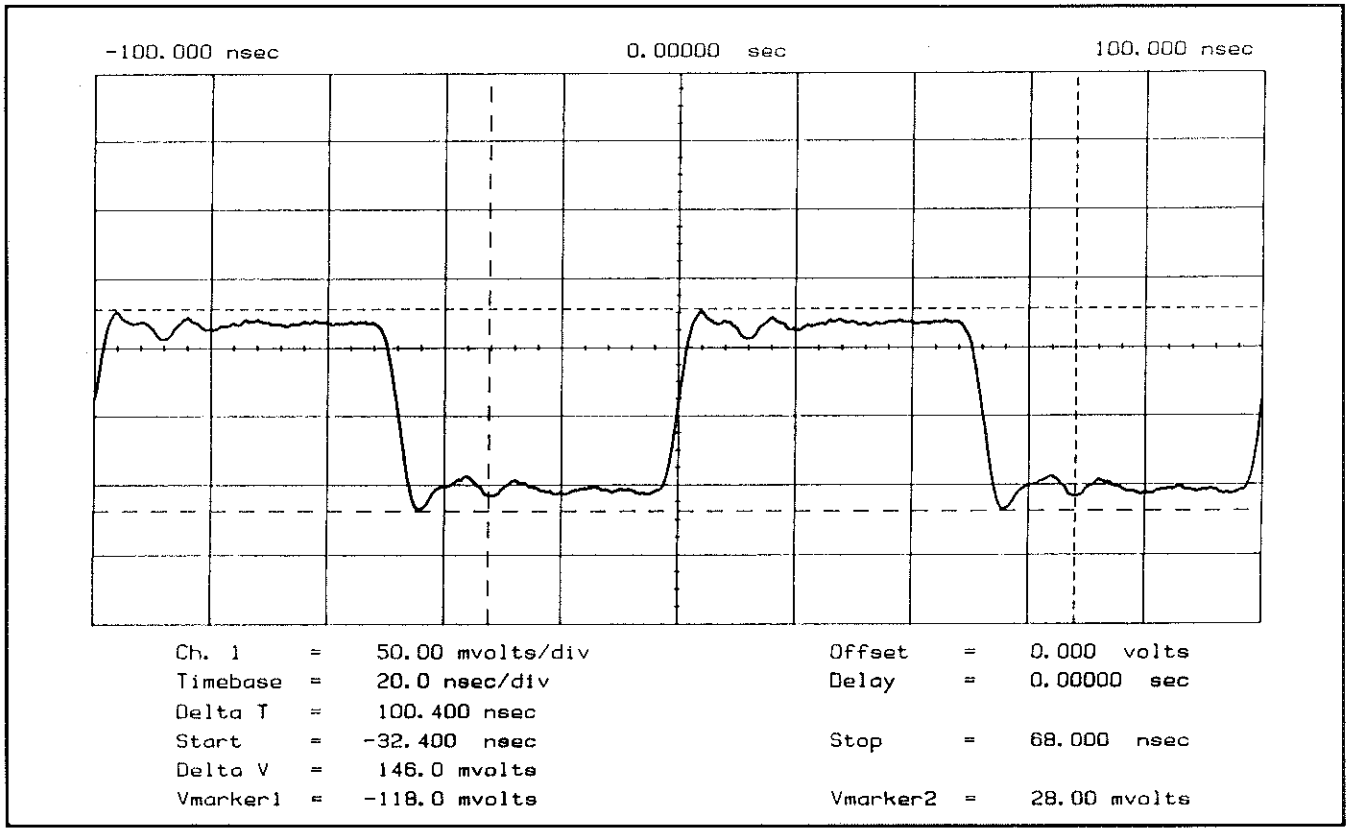


Figure 7C-8. Comparator Input Pin A2U4(3) [A2U15(3)] Waveform

C. Observe A2U4(3) [A2U15(3)]. While in MANUAL trigger mode, vary the level and observe the signal as its dc level shifts. The Comparator's output always switches at the zero crossing point. Changing the point at which the Comparator triggers is controlled by the DC Offset Hybrid when it shifts the dc level of the input signal.

D. Measure A2U2(4) [A2U14(4)] DC Offset Hybrid input pin. It should measure 1 Vp-p.

E. Measure Comparator Hybrid output pin A2U4(13) [A2U15(13)]. This point should measure 0.9 Vp-p nominal. (The gain of the Comparator Hybrid is somewhat less than unity). The A2U4 [A2U14] Comparator output pin is a EECL-level digital signal that varies between 0V and –0.8 V *nominal.*

F. If the signal is observed, replace A2U4 [A215].

G. Nominal signal levels of the Comparator Hybrid ICs, A2U4 [A2U15], are listed in *Table 7C-2.*

Table 7C-2. Comparator Hybrid IC Pin Voltages

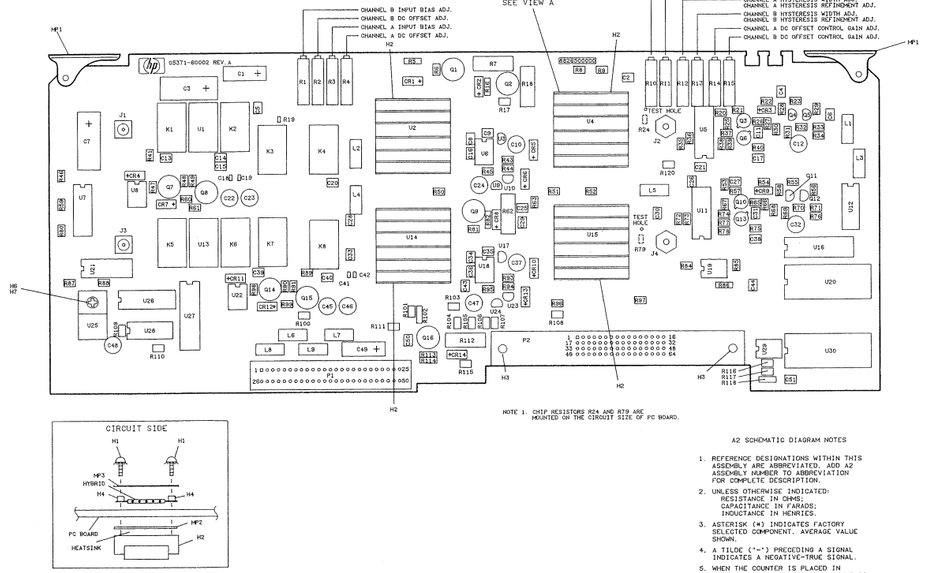
Pins	Signal
1	+15V dc
2	GND
3	Input Signal
4	GND
5	–15V dc
6	No Connection
7	0V
8	+5V dc (Adjustable)
9	No Connection
10	No Connection
11	–5.2V dc
12	GND
13	Output Signal
14	No Connection
15	GND
16	–15V dc
17	–8V dc (Adjustable)
18	+100 mV
19	+15V dc
20	–5.2V dc

7C-21. Trigger Level Control Check

(The triggering voltage entered from the front panel is in digital form. Therefore, U20 converts it into analog form and passes it through a unit inverter, U19.)

A. Set trigger level voltage to +480 mV.

B. Verify that the analog output of D/A Converter, A2U20(9) [A2U30(9)], and the output of operational amplifier A2U19 [A2U29] is approximately –480 mV. If these two voltages differ, operational amplifier, A2U19 [A2U29], is malfunctioning. Replace A2U19 [A2U29]. However, if these two voltages approximate one another but do not equal –480 mV, the D/A Converter, A2U20 [A2U30], is malfunctioning. Replace A2U20 [A2U30].



A2 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A2 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. WHEN THE COUNTER IS PLACED IN COMMON MODE, THE SIGNAL AT INPUT IS ROUTED TO CHANNEL B DC OFFSET HYBRID VIA K4 AND K8; THERE THE SIGNAL IS TERMINATED INTO 50 OHMS.
6. ELECTRICALLY, U4(11) IS CONNECTED TO THE SAME NODE AS U5(11).
7. THIS NODE SUPPLIES POWER TO U11 AND CHANNEL B SYNC COMPARATOR U15.
8. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

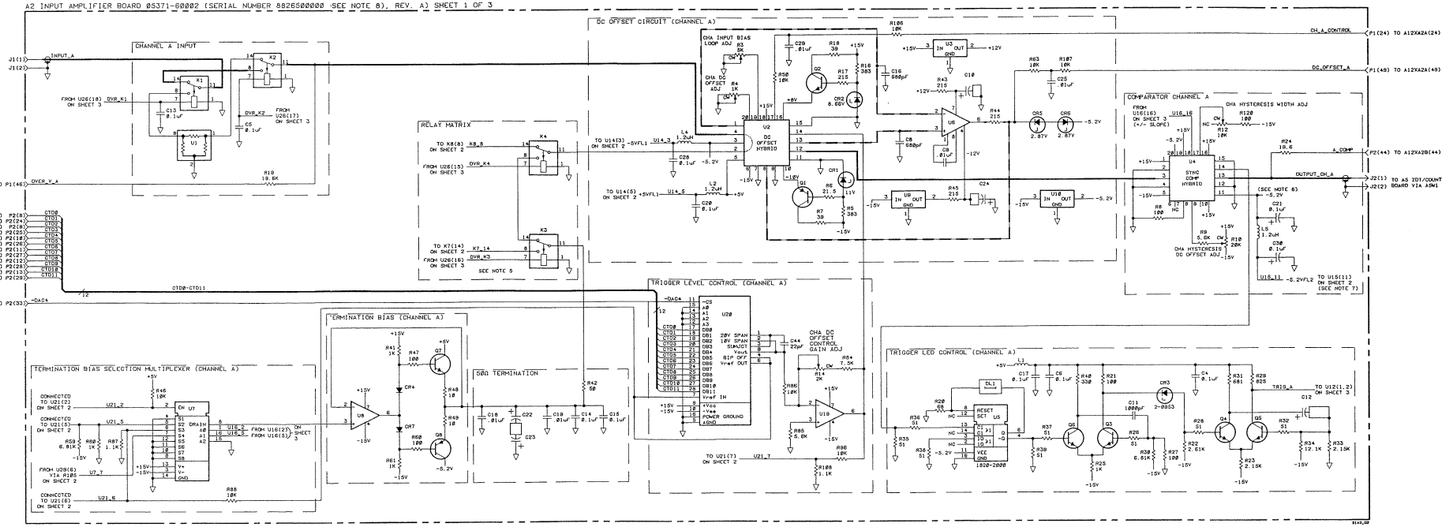
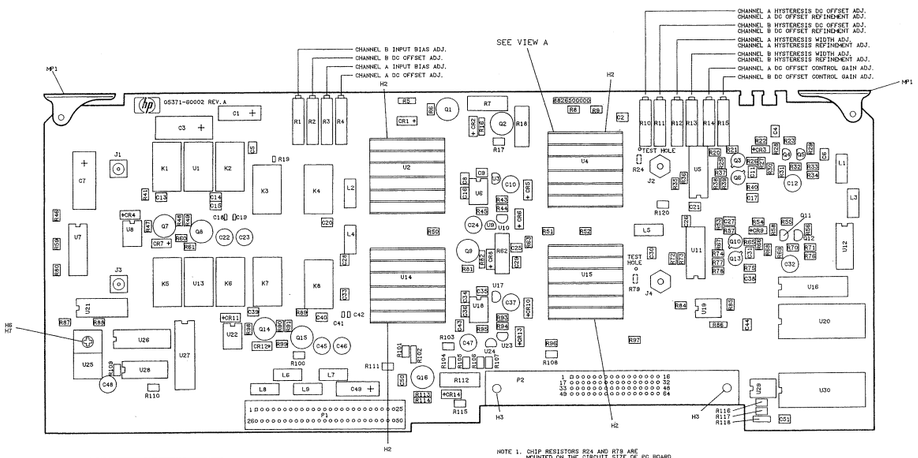


Figure 7C-9. A2 Input Amplifier Board, Schematic Diagram (Sheet 1 of 3)



NOTE 1. CHIP RESISTORS R24 AND R79 ARE MOUNTED ON THE CIRCUIT SIDE OF PC BOARD.

A2 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A2 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. WHEN THE COUNTER IS PLACED IN COMMON MODE, THE SIGNAL AT INPUT IS ROUTED TO CHANNEL B DC OFFSET HYBRID VIA K4 AND K8. THERE THE SIGNAL IS TERMINATED INTO 50 OHMS.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

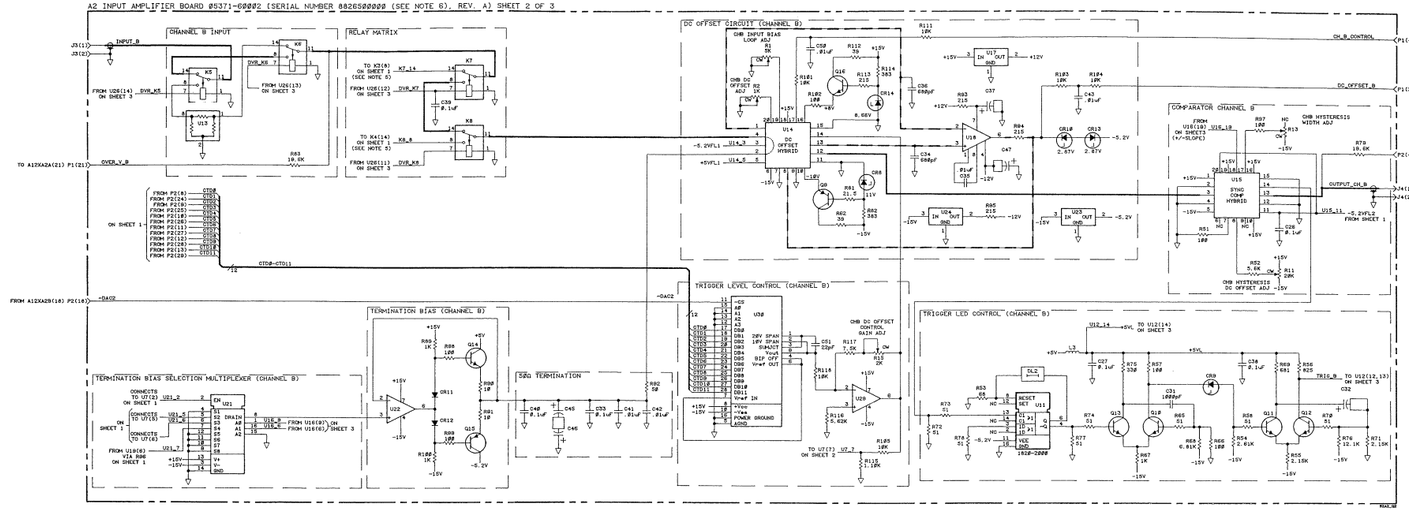
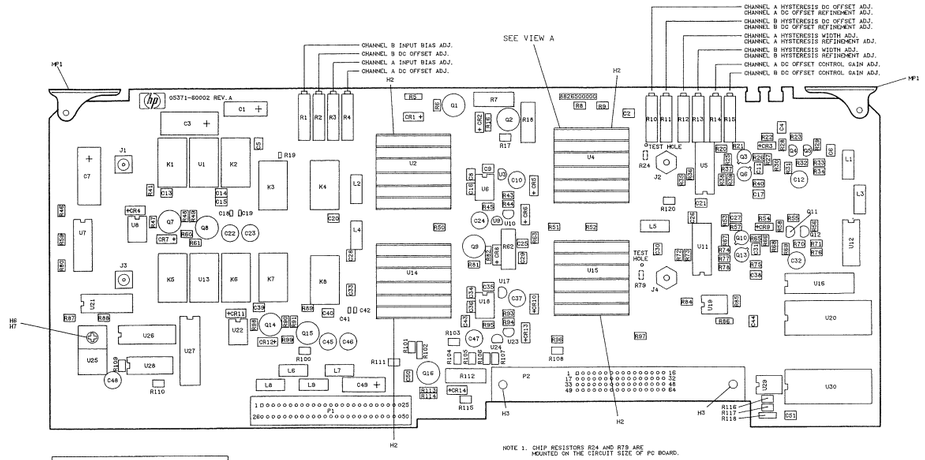
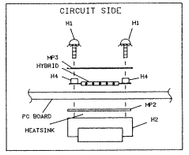


Figure 7C-9. A2 Input Amplifier Board, Schematic Diagram (Sheet 2 of 3)



NOTE 1. CHIP RESISTORS R24 AND R78 ARE MOUNTED ON THE CIRCUIT SIDE OF PC BOARD.



VIEW A

A2 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A2, A8, A11, OR A12 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

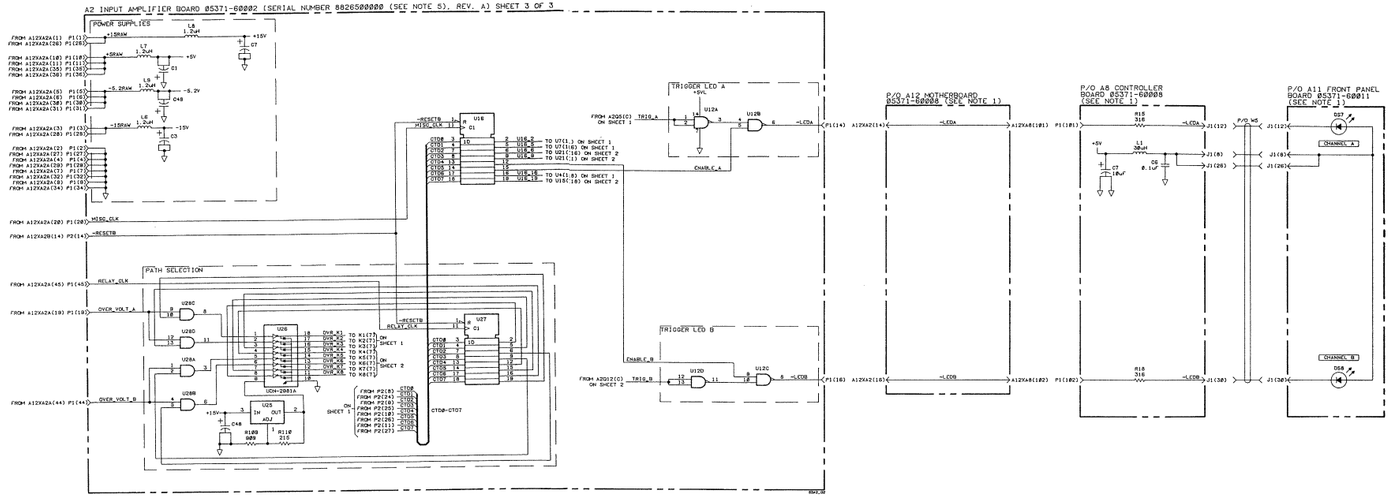


Figure 7C-9. A2 Input Amplifier Board, Schematic Diagram (Sheet 3 of 3)

7D A4 INTERPOLATOR

SECTION 7D
A4 INTERPOLATOR BOARD

7D-1. A4 INTERPOLATOR BOARD

7D-2. Introduction

The A4 Interpolator Board permits time interval measurements with resolution of 200 ps. This is accomplished by using accurate copper-etched printed circuit board delays ("D1", "D2", ... , and "D9") configured to detect coincidence between the start event and stop event pulses, IT1 and IT2 respectively, and the 500 MHz reference timebase (CLKA). The amount of delay detected by each interpolator is encoded as a 4-bit, TTL-level binary code and is used with accumulated timebase data accumulated by the A5 ZDT/Count Board Timing Counter to generate a measurement gate time having a resolution of 200 ps. The main functions of the interpolator can be summarized as follows:

- Resolves Start and Stop (IT1 and IT2) event pulse times to multiples of 200 ps.
- Generates CI1 to latch the A5 ZDT/Count Board Timing Counter counting 2 ns intervals.
- Generates CI2 to latch the A5 ZDT/Count Board Timing Counter.
- Generates a 4-bit, TTL-level binary code equivalent to the measured time difference between the event-edge trigger (IT1 and IT2) and the 500 MHz reference timebase (CLKA).

The A4 assembly has two identical interpolator circuits; Interpolator 1 (Start) and Interpolator 2 (Stop). Single-channel measurements use Interpolator 1 for the measurement start and Interpolator 2 for the measurement stop. For dual channel measurements, Interpolator 1 is used to resolve the start of the gate, while Interpolator 2 is used to resolve the stop of the gate. The following theory refers to Interpolator 1 (Start) but can be applied to Interpolator 2 (Stop) as well. See "A4 Interpolator Board Block Diagram" in *Figure 7D-1* for reference.

7D-3 A4 Interpolator Operation Overview

When the HP 5371A performs a Time Interval measurement, there is an inherent ± count uncertainty introduced by opening and closing the counting gate. Usually the gate, as defined by Start (IT1) and Stop (IT2) event pulses, does not open or close at the same time the positive edge of the 500 MHz timebase pulse occurs. The A5 ZDT/Count Board Timing Counter ZDT chain counts the integral number of 500 MHz reference timebase pulses while the counting gate is open. The A4 Interpolator 1 (Start) and Interpolator 2 (stop) circuits synchronize the 500 MHz reference timebase to the asynchronous Start and Stop event pulses, IT1 and IT2, and measure the fractional time difference between the positive edge of the first and last gated event pulse and the next positive-edge of the 500 MHz reference timebase pulse. This process increases the HP 5371A's time resolution tenfold without increasing the instrument's timebase frequency. The A5 Sequencer IC (A5U29) sends the "Start" event pulse, IT1, to the interpolator board, where it is synchronized with the 500 MHz reference timebase (CLKA). For each IT1 pulse received, the *Synchronizer* stage outputs an IT and CI pulse. The relative timing of these two pulses correspond in time to the original IT1 and the next 500 MHz clock edge to follow IT1. IT and CI edges propagate down a pair of controlled transmission lines through a chain of high-speed, edge-triggered flip-flops located in the *10-Stage Flash Interpolator Chain* stage. The CI edge clocks all the flip-flops, and the IT signal drives the data input of the flip-flops. Between consecutive flip-flops, the IT signal is delayed 200 ps relative to CI. IT led CI by up to 2 ns (10 × 200 ps) when the two signals entered the chain. As the two edges propagate down the chain, IT loses this lead in 200 ps increments. The flip-flops compare the phases of CI and IT. If IT leads CI at a given flip-flop, that flip-flop latches a logical "one". If IT lags CI, the flip-flop latches a logical "zero". The outputs of the flip-flops form a "thermometer" code representative of the time by which IT originally led CI. After passing through the entire chain, CI is terminated, and IT is sent to A4U3 to reset the *Synchronizer* stage. A copy of the synchronized latch CI, called CI1, is sent to the

A5's Timing Counter ZDT chain to initiate the Timing Counter's integral count process. The current value of the Timing Counter is stored in its corresponding measurement RAM. The A4 circuits detect and encode the point of coincidence between the "Start" event pulse, IT1, and the 500 MHz reference timebase, CLKA. This 4-bit, TTL-level binary code is sent to the A6 DMA/Gate Board and temporarily stored in the "Start" Interpolator RAM, A6U37. This process is repeated for the Sequencer's "Stop" event pulse, IT2.

Then, under A7 Processor Board control, the start and stop interpolation results and the A5 ZDT/Count Board's Timing Counter RAM integral count data are read from memory and either stored in the A7 processor RAM area or the raw binary data is "dumped" directly to the HP-IB interface via the A8 I/O Controller Board. The A7 68000 microprocessor or an external controller can then determine the actual gate time factor for calculating the time interval, thus eliminating the ±1 count uncertainty. (See *Figure 7D-1.*) By using this interpolation process, resolution of gate times can be improved from 2 ns to multiples of 200 ps.

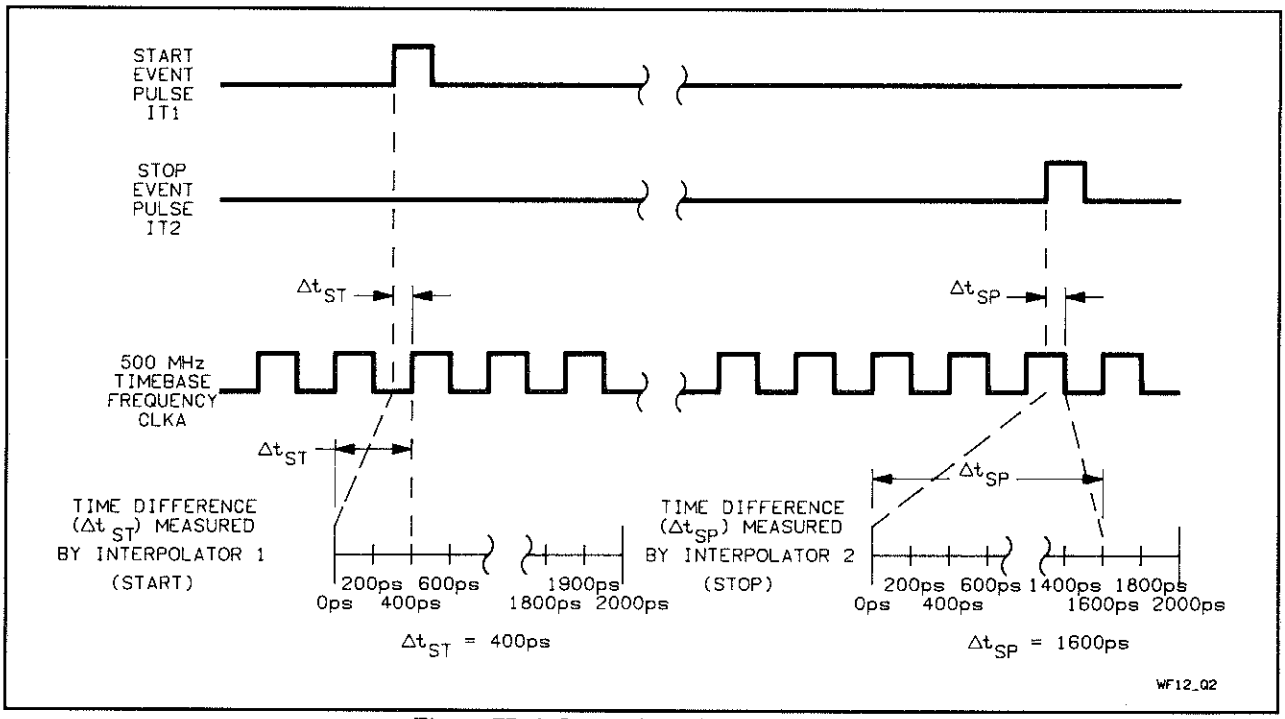


Figure 7D-1. Interpolator Timing Diagram

7D-4. 500 MHz Splitter

Both interpolator circuits require a 500 MHz reference timebase. The 500 MHz signal, CLKA, is supplied by the A14 Timebase Multiplier Board. The splitter's resistive divider network comprised of A4R51, R53 and R54, preserves the 50Ω loading of the 500 MHz source and supplies Interpolator 1 (Start) and Interpolator 2 (Stop) circuits with a 500 MHz reference timebase input. The 500 MHz is distributed to both interpolators over matched length transmission lines. Equal time delay paths through both circuits is necessary for proper timebase latching.

7D-5. Synchronizer

Time Interval measurements are defined by a start pulse (IT1) and a Stop pulse (IT2). The IT1 and IT2 pulses are not synchronous with the 500 MHz reference timebase, so there is some fraction of a clock-cycle which occurs between the positive edge of each of these pulses and the next positive edge of the 500 MHz reference timebase. This fraction of a cycle is between 0 and 2.0 ns long. The overall function of the A4 Interpolator is to measure the time of these fractional clock-cycles. The *Synchronizer* stage receives an IT1 (or IT2) pulse from the Sequencer IC (A5U29), selects the next positive of the reference timebase, and outputs two positive edges which are spaced in time as IT1 and the reference timebase. The two edges, IT and CI, then propagate through the *10-Stage Flash Interpolator Chain.*

The 500 MHz reference timebase continuously clocks flip-flops A4U1 and U2. When a "Start" event pulse (IT1) occurs, flip-flop A4U2 arms and its output goes high at the next positive clock edge. But since the IT1 pulse is asynchronous (i.e., it can occur at any time relative to the clock phase), occasionally the A4U2 output will float in a metastable state (i.e., teeter), unable to determine whether the IT1 edge arrived before or after the clock edge. Flip-flop A4U2 drives the data input of A4U1. A delayed version of the clock drives A4U1. This allows A4U2 to teeter for up to approximately 1 clock pulse width (2 ns) before its output is clocked into A4U1. The resulting output of A4U1 is CI. Flip-flop A4U3 ensures that the path from IT1 to IT is the same length as the path from the *500 MHz Splitter* stage to CI. Potentiometer A4R6 permits balance adjustment of the CI and IT path delays. A4U3 also uses its own IT signal, after it has been delayed by 2 ns in the *10-Stage Flash Interpolator Chain* stage, to reset the *Synchronizer* stage.

7D-6. GATE 1 Output EECL-to-ECL Inverter

One of the signals generated by the *Synchronizer* stage is GATE 1. Gate 1 is a copy of the IT1 pulse, which is generated by the A5 assembly's Sequencer IC after all arming conditions for a particular measurement have been met. Gate 1 indicates the start of a measurement sample. Gate 1 is generated by flip-flop A4U3, pin 4. From here the signal is inverted and shifted to TTL logic levels by common-emitter amplifier A4Q4 of the *Gate 1 Output EECL-to-TTL Inverter* stage. Gate 1 drives buffer A12U5C located on the A12 Motherboard. The buffer, in turn, drives the rear-panel GATE 1 output BNC at TTL voltage levels.

7D-7. CI1 EECL-TO-ECL Inverter and Selectable Delay

Signal ~CI, generated by the *Synchronizer* stage, is inverted and level shifted by cascaded common-emitter amplifier, A4Q1 and Q4, and common-collector amplifier, A4Q2, providing an ECL positive-edge signal, CI1. Jumpers A4W1 through A4W5 comprise the selectable delay circuit. This circuit allows ensures that CI leads the 500 MHz clock edge by 750 ± 700 ps as measured at ZDT counter A5U28. A4W2 and W3 are loaded at the factory for a nominal delay of 660 ps, which yields the proper CI-to-500 MHz delay of 750 ps measured under nominal conditions. CI1 is sent to the A5 ZDT/Count Board's Timing Counter ZDT3A, A5U28, triggering it to begin counting the 2 ns timebase pulses.

7D-8. 10-Stage Flash Interpolator Chain

This circuit measures the time between the synchronized CI to IT edges. The 2 ns period of the reference timebase is divided into 10 sub-periods. Each sub-period is detected by one of nine D-type flip-flops (A4U4, U5, U7, U8, U10, U12, U14, U15, and U17) of the *10-Stage Flash Interpolator Chain*. Imagine a race down the interpolator chain between signals CI and IT, where after each stage of comparison, the IT pulse is given a data-to-timebase 200 ps increment of delay. The two signals are then again compared at the next flip-flop stage. Therefore, signals IT and CI are traveling down two parallel paths having nine D-type flip-flops at set time intervals along this path. IT is delayed after every flip-flop by 200 ps so that IT is sequentially walked through the 2 ns in 200 ps steps. The phase comparison is performed by flip-flops which are clocked by the CI signal and use IT as the data input. If IT reaches a given flip-flop before CI, the flip-flop is clocked with a logical "one" (see *Figure 7D-2*). Conversely, if IT reaches a given flip-flop after CI, the flip-flop is clocked with a "zero" (see *Figure 7D-3*). The output of all nine flip-flops logically combine to form an EECL-level "thermometer" code. For example, if an 1800 ps start delay is detected, flip-flop A4U17 output is set at a logical "one" while flip-flops A4U3-5, U7, U8, U10, U12, U15, and U14 are set at "logical zeros". Likewise, if a 0 ps delay is detected, all the flip-flops in the interpolator chain are programmed at a logical "one". The "Q" output of one flip-flop is then wire-ANDed with the "~Q" output of the following flip-flop, generating a one-hot code that corresponds to the "thermometer" code output.

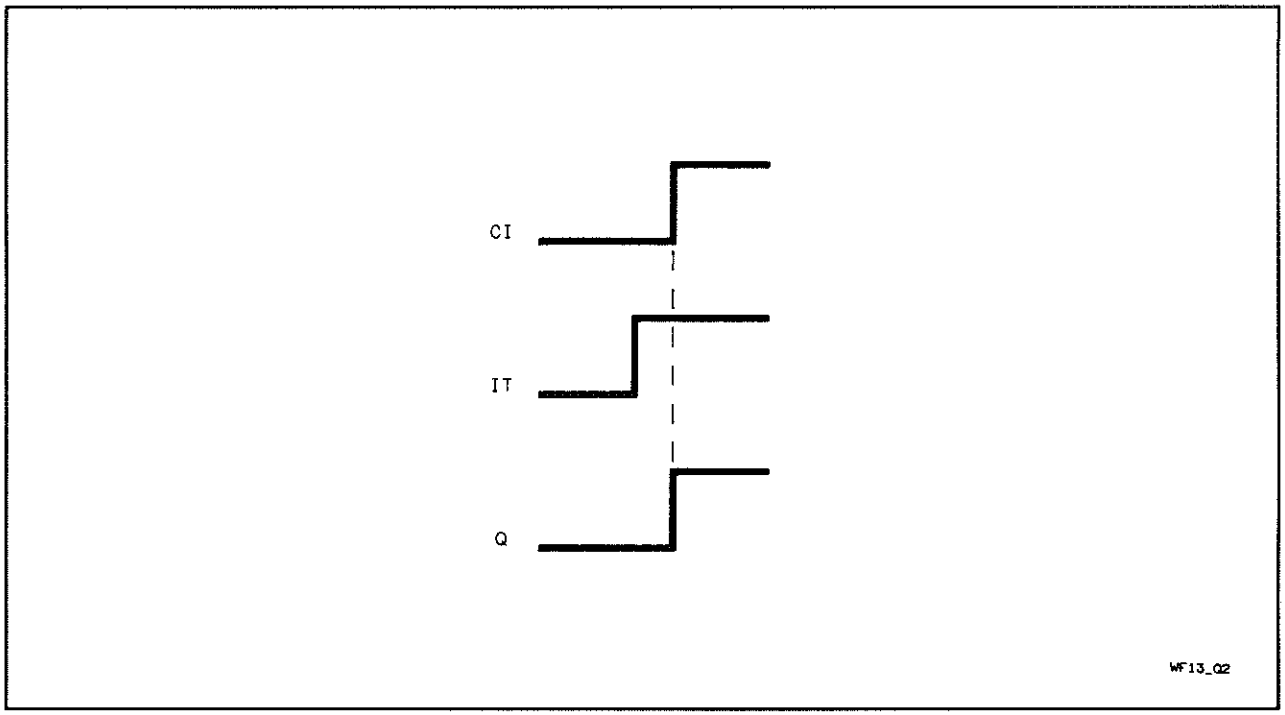


Figure 7D-2. IT Leading C1

Adjustment of potentiometers A4R19, R20, R24, R27, R31 and R46, which are located on the timebase input of each flip-flop stage, eliminate any offsets that may exist between the timebase input CI and data input IT. By adjusting these pots, the propagation delay differences between the IT and CI flip-flops are zeroed, thus improving interpolator linearity.

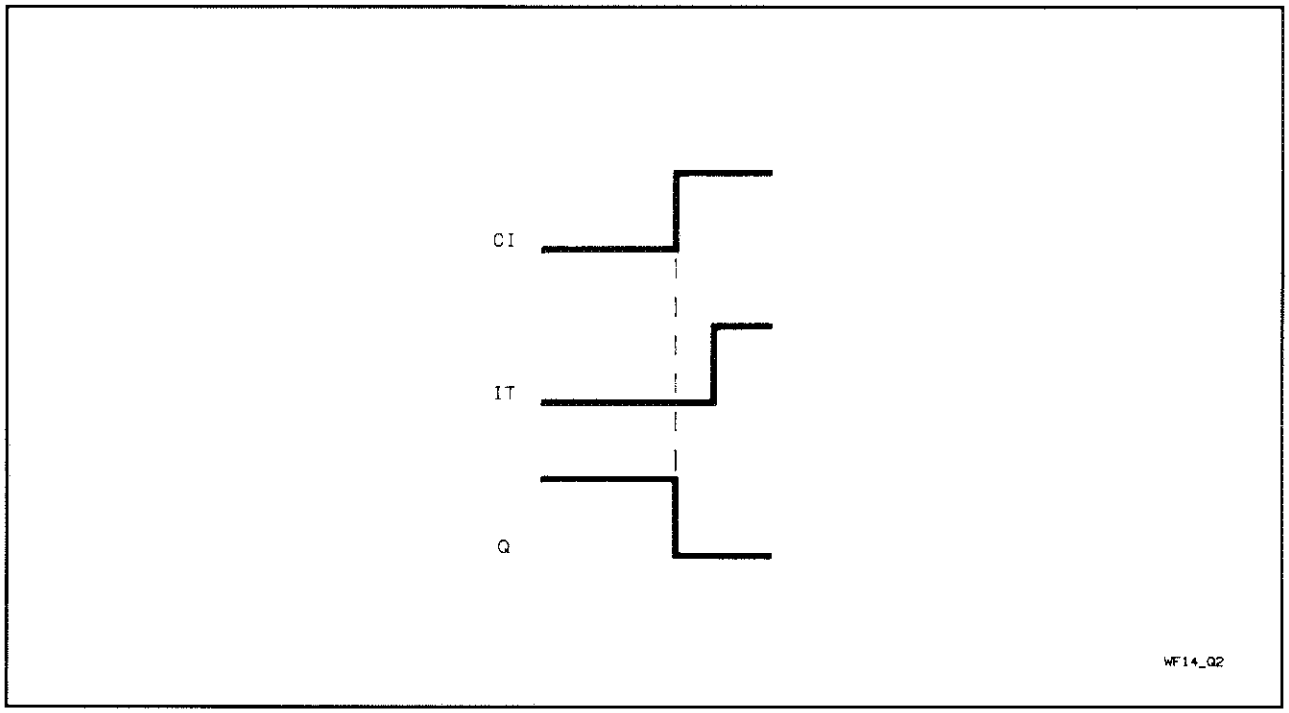


Figure 7D-3. IT Lagging C1

7D-9. One-Hot-To-Binary Encoder

The *One-Hot-To-Binary Encoder* encodes the one-hot code to an ECL level binary number equivalent to the delay detected by the interpolator chain. Transistors A4U6ABCD, U9ABCD, U11ABCD, and U13ABC detect the cross-over point between logical "ones" and "zeros" at the outputs of the flip-flop chain and translate this information into a single-bit, ECL level "one-hot" code. For example, if flip-flops A4U3-5, U7, U8, and U10 are set at logical "zero" and flip-flops A4U12, U14, U15, and U17 are set at logical "ones", bits INTST3 and INTST4 are asserted while bits INST2 and INST5 remain at logical "zero". As shown in the previous example, if flip-flop A4U16 (pin 6) is asserted, the ECL-to-TTL Translator's (A4U16) outputs would be a 4-bit binary 0101. This is the binary equivalent of a interpolated delay of 1000 ps (D1 + D2 + D3 + D4 + D5 = 200 ps + 200 ps + 200 ps + 200 ps + 200 ps = 1000 ps). This digital information, comprised of signals INTST2, INTST3, INTST4 and INTST5, is sent to the A6 DMA/Gate Board's *Start Interpolator* RAM for temporary storage.

7D-10. ECL-to-TTL Translator

Translator A4U16 converts the 4-bit, ECL-level binary code "Start" interpolation result to TTL-level signals (INST2, INST3, INST4 and INST5) and provides the current to drive latch A6U54 located on the A6 DMA/Gate Board. Transistor A4U13D and passive components A4R44, R42, C26 and C28, provide –1.04 reference Volts to A4U16.

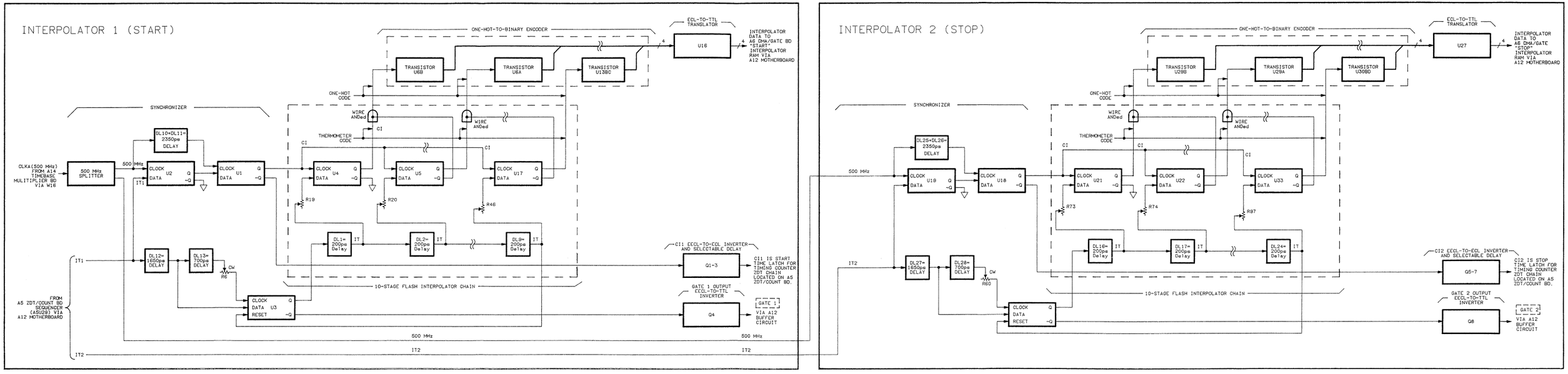


Figure 7D-4. A4 Interpolator Board Block Diagram

7D-11. A4 Interpolator Board Troubleshooting

7D-12. TEST EQUIPMENT REQUIRED

- HP 54100A Digitizing Oscilloscope (or equivalent)
- HP 8656A Signal Generator or HP 8662A Signal Generator

7D-13. DIAGNOSTICS

- Diagnostic Test 5. Count ICs
- Diagnostic Test 21. Calibrate Interpolators

7D-14. BACKGROUND

The A4 Interpolator Board, HP Part Number 05371-60004, provides the HP 5371A with the ability to resolve measurements down to 200 ps. Without the A4 assembly, the 5371A would only be able to resolve measurements down to 2ns. The Interpolator Board is made up of two identical circuits: Interpolator 1 (start) and Interpolator 2 (stop). When viewed from the component side, Interpolator 1 is the left half of the board; the right half is Interpolator 2.

	EECL	ECL	TTL
Logic 1	0 V	–0.8 V	5 V
Logic 0	–0.5 V	–1.7 V	0 V

7D-15. A4 TROUBLESHOOTING APPROACH

To troubleshoot the A4 assembly, you must first isolate the failure to Interpolator 1 or Interpolator 2. The signals are then traced back to the failed component.

7D-16. A4 FAILURE SYMPTOMS

A. Apply a 10 MHz, 1 Vp-p, square wave to the 5371A front panel CHANNEL A input. Use an external source for this quick check.

B. Press 5371A front-panel PRESET key. If the A4 assembly has failed, the displayed result will read worse than 100ns ± 2ns. In addition, the following symptoms may also be observed:

- Measurement accuracy is reduced to 2ns or worse.
- Measurement readings are unstable and frequently erroneous.
- Diagnostic Test 5, "Count ICs", will indicate a failure with ZDT3A and ZDT3B if these ZDT Counters do not receive the CI1 and CI2 latch signals from the A4 assembly.

7D-17. A4 TROUBLESHOOTING PREPARATION

C. Place the A4 Interpolator Board on the A19RF Extender Board, HP Part Number 05371-60016.

D. Disconnect the 500 MHz reference frequency from the A4J2 connector.

E. Apply a +10 dBm 499.9833 MHz signal from an HP 8656A to the A4J2 connector.

F. Connect the 10 MHZ STANDARD FREQUENCY OUTPUT of the 5371A to the 8656A rear-panel timebase input (INPUT). (This will synchronize the timebase clocks of the two instruments.)

G. Connect a BNC cable from the 5371A rear-panel 10 MHZ STANDARD FREQUENCY OUTPUT connector to the 5371A CHANNEL A input pod.

H. Set 5371A STBY-ON power switch to ON.

I. Press TEST key on the 5371A front panel. Select Diagnostic Test 21, "Calibrate Interps". Press the Run softkey.

J. Change the frequency output of the HP 8656A with the fine-tuning knob located on its front panel. Adjust the frequency until only one bar is seen in each column displayed on the 5371A screen.

K. Remove the W6 DMA Cable (HP Part Number 05371-60204) from the top edge of the A6 DMA/Gate Board. (This places the 5371A count hardware in a free-run state.)

L. Using the FUNCTION menu, set the 5371A to measure TIME INTERVAL in AUTOMATIC Arming Mode.

7D-18. A4 TROUBLESHOOTING PROCEDURE

NOTE

The timing diagrams located at the end of this procedure were generated using a digitizing oscilloscope. All measurements are made using a 50W 10:1 divider probe.

7D-19. Interpolator 1 (Start)

A. Using an oscilloscope, verify the presence of the GATE 1 signal (*Figure 7D-5*) at the 5371A rear-panel output. If the signal is bad, trace the failure back through A4Q4, then to A4U3(4) (EECL level), then to the IT1 signal (*Figure 7D-6*) at A4P2(1).

B. Verify the presence of CI1 at A4P4(1)(TP1), see *Figure 7D-7*. If the signal is bad, trace the failure back through A4Q1-A4Q3, then to A4U1(4) (see *Figure 7D-8*), then to A4U2(6). Verify that the START_SYNC_500MHz signal is present at A4U2(13).

C. Verify the presence of the CI (TP4) (*Figure 7D-9*) and IT (TP3) (*Figure 7D-10*) signals at A4R21 and A4R19 (near A4U4). If these signals are bad, trace the failure back through A4U1 - A4U3.

NOTE

Refer to the component locator found with the A4 schematics for all Test Point (TP) locations.

D. Verify the presence of an output at A4U4(6) (see *Figure 7D-11*), A4U5(6), A4U7(6), A4U8(6), A4U10(6), A4U12(6), A4U14(6), A4U15(6) and A4U17(6).

E. Verify the presence of a signal at A4U16(3,7,11,15). If any one of those signals are bad, then trace the failure to one of the following transistor packs: A4U6, A4U9, A4U11, or A4U13. See *Figures 7D-12* through *7D-14*.

NOTE

Note that the period of the signal at A4U16(7) is approximately 60 microseconds.

F. Verify that the outputs of A4U16(4,5,12,13) are the same as their respective inputs, A4U16(3,7,11,15), in step 5. See *Figures 7D-12* through *7D-14*.

G. If the signals in Steps 1 through 6 are good, then proceed to section B, the Stop Interpolator.

7D-20. Interpolator 2 (Stop)

A. Using an oscilloscope, verify the presence of the GATE 2 signal (see *Figure 7D-5*) at the 5371A rear-panel output. If the signal is bad, trace the failure back through A4Q8, then to A4U20(4) (EECL level), then to the IT2 signal (see *Figure 7D-6*) at A4P6(1).

B. Verify the presence of CI2 at A4P3(1) (TP2) (see *Figure 7D-7*). If the signal is bad, trace the failure back through A4Q5 - A5Q7, then to A4U18(4) (see *Figure 7D-8*), then to A4U19(6). Lastly, verify the presence of the STOP_SYNC_500MHz signal at A4U19(13).

C. Verify the presence of the CI (TP6) (see *Figure 7D-9*), and IT (TP5) (see *Figure 7D-10*), signals at A4R75 and A4R73 (near A4U21). If these signals are bad, trace the failure back through A4U18 - A4U20.

D. Verify the presence of an output at A4U21(6), A4U22(6), A4U23(6), A4U24(6) A4U25(6), A4U26(6), A4U28(6), A4U31(6) and A4U33(6). See *Figure 7D-11*.

E. Verify the presence of a signal at A4U27(3,7,11,15). If any one of those signals are bad, then trace the failure back to one of the following transistor packs: A4U29, A4U30, A4U32 or A4U34. See *Figures 7D-12* through *7D-14*.

F. Verify that the outputs of A4U27(4,5,12,13) are the same as their respective inputs, A4U27(3,7,11,15), in step 5. See *Figures 7D-12* through *7D-14*.

G. If the signals in steps 1 through 6 are good, then the A4 Interpolator board is probably good.

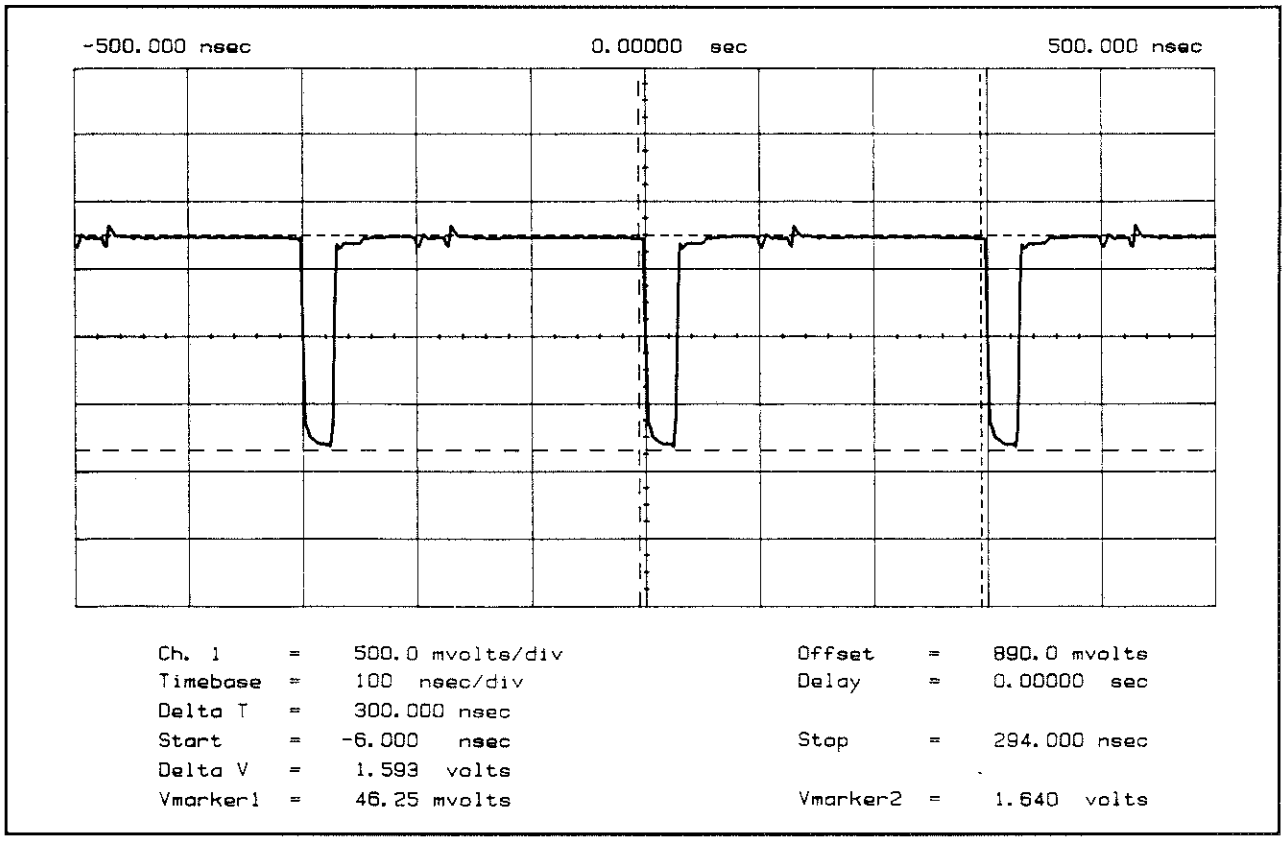


Figure 7D-5. GATE 1 and GATE 2 Signals at Rear Panel

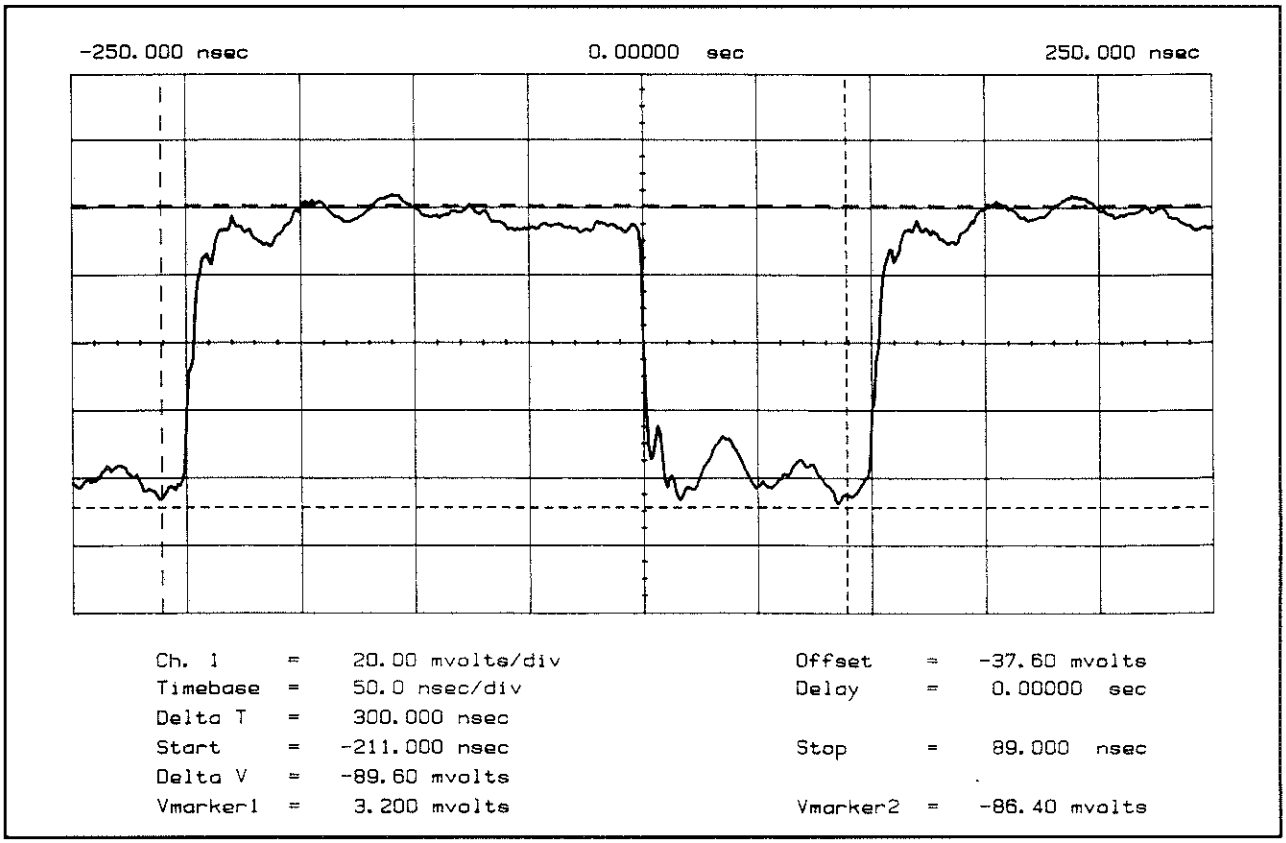


Figure 7D-6. IT1 and IT2 Waveforms

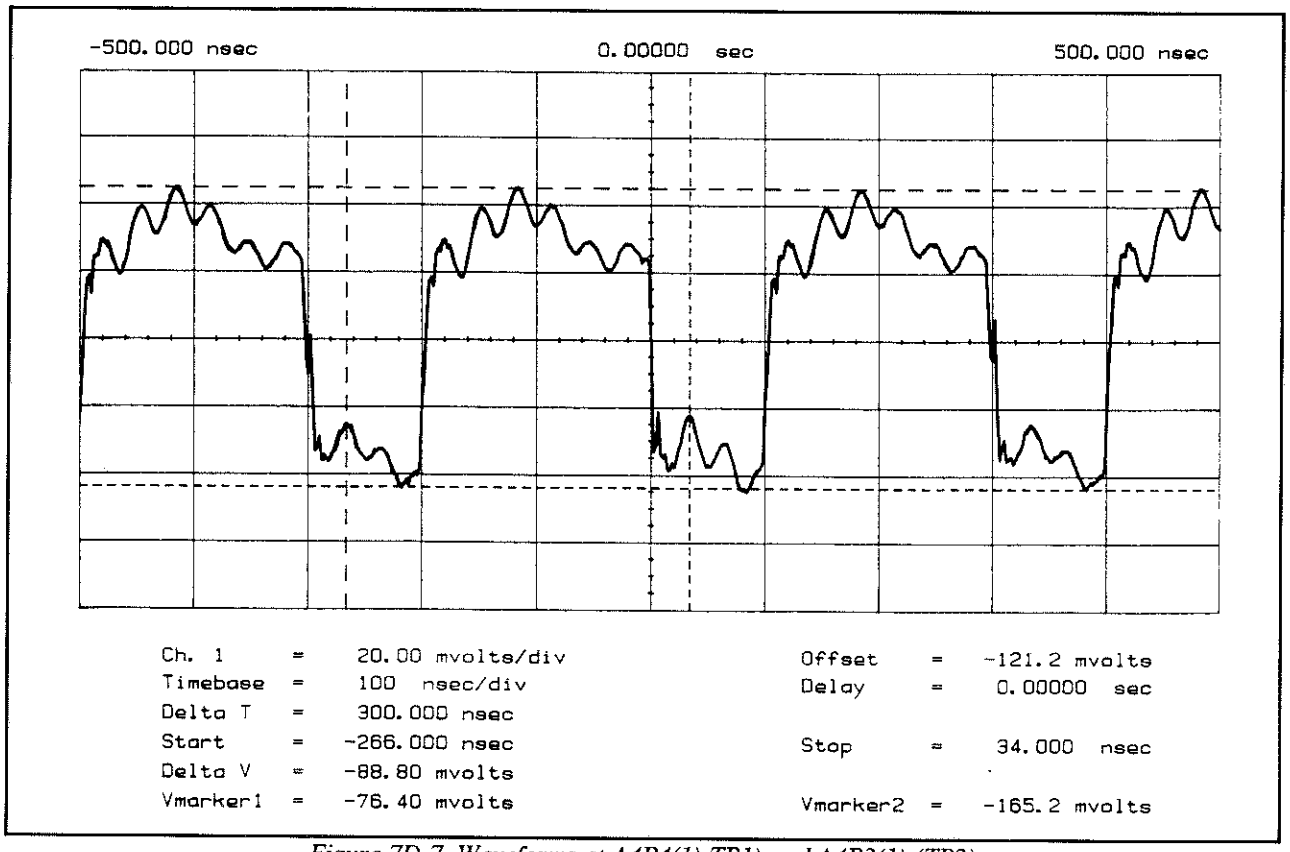


Figure 7D-7. Waveforms at A4P4(1) TP1) and A4P3(1) (TP2)

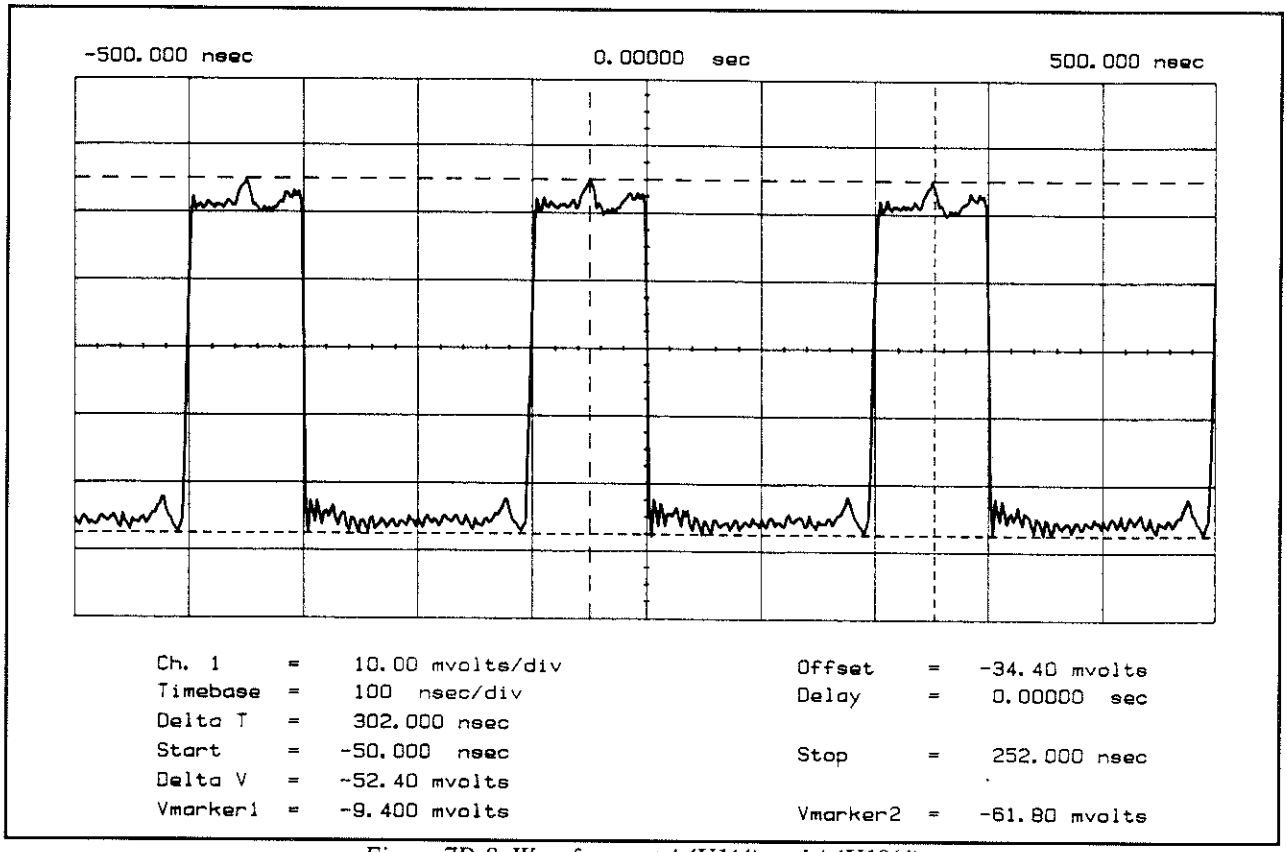


Figure 7D-8. Waveforms at A4U1(4) and A4U18(4)

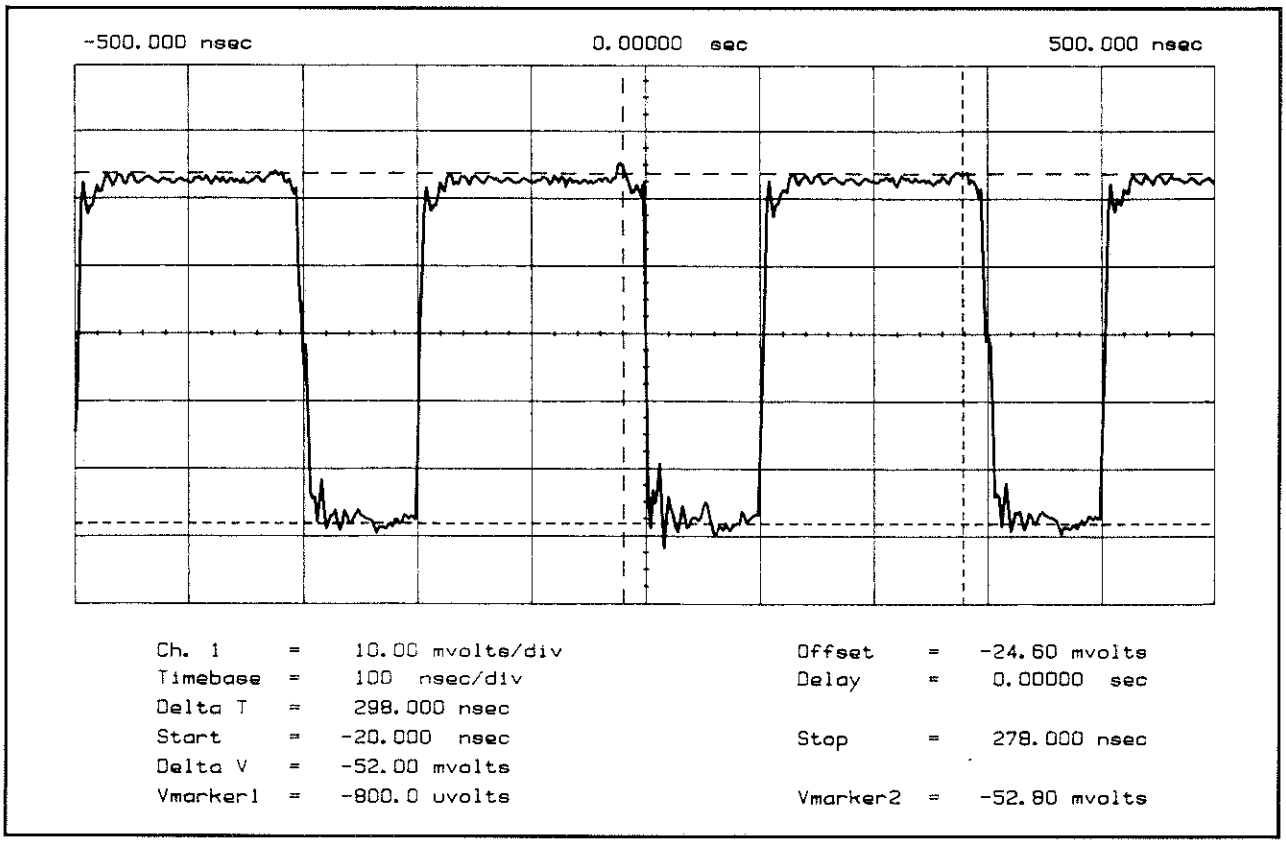


Figure 7D-9. Waveforms at TP4 and TP6

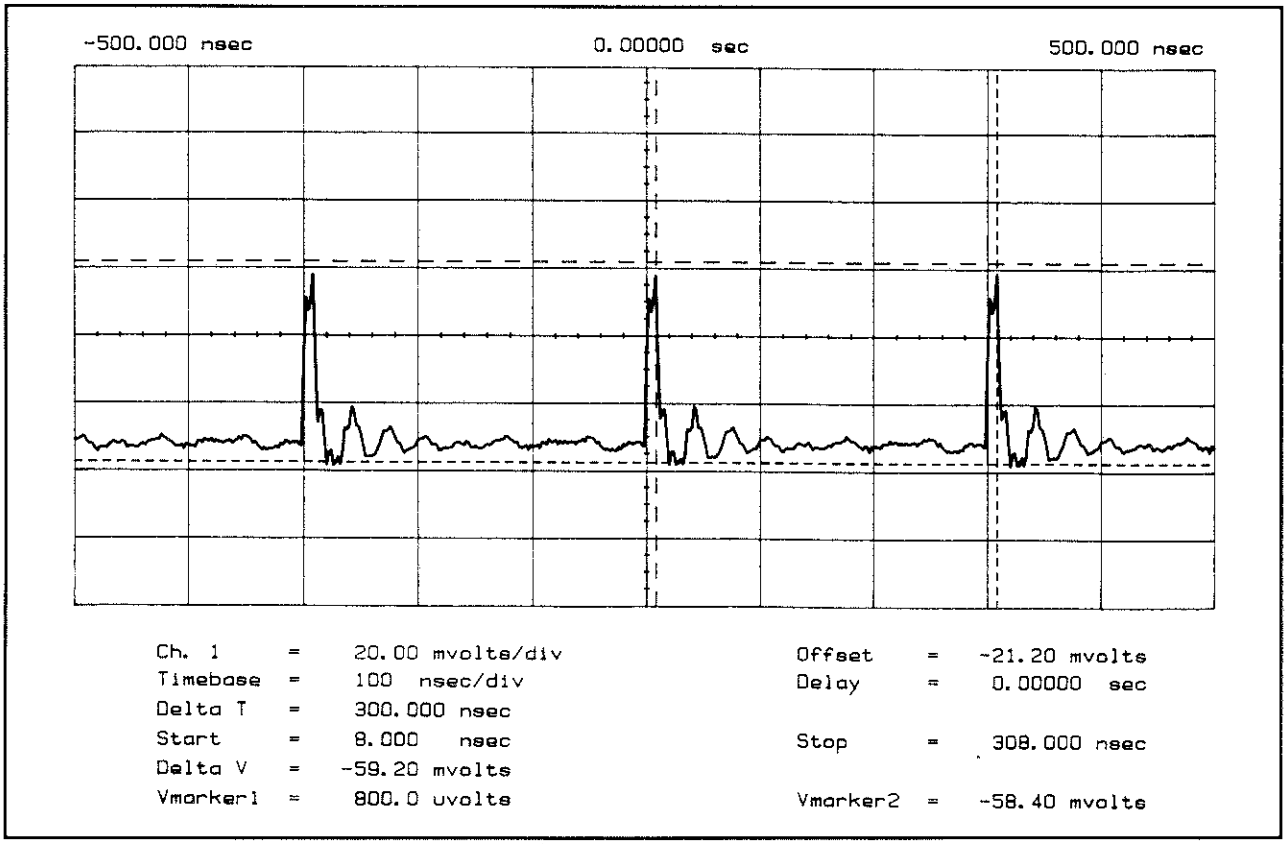


Figure 7D-10. IT1 (TP3) and IT2 (TP5) Waveforms

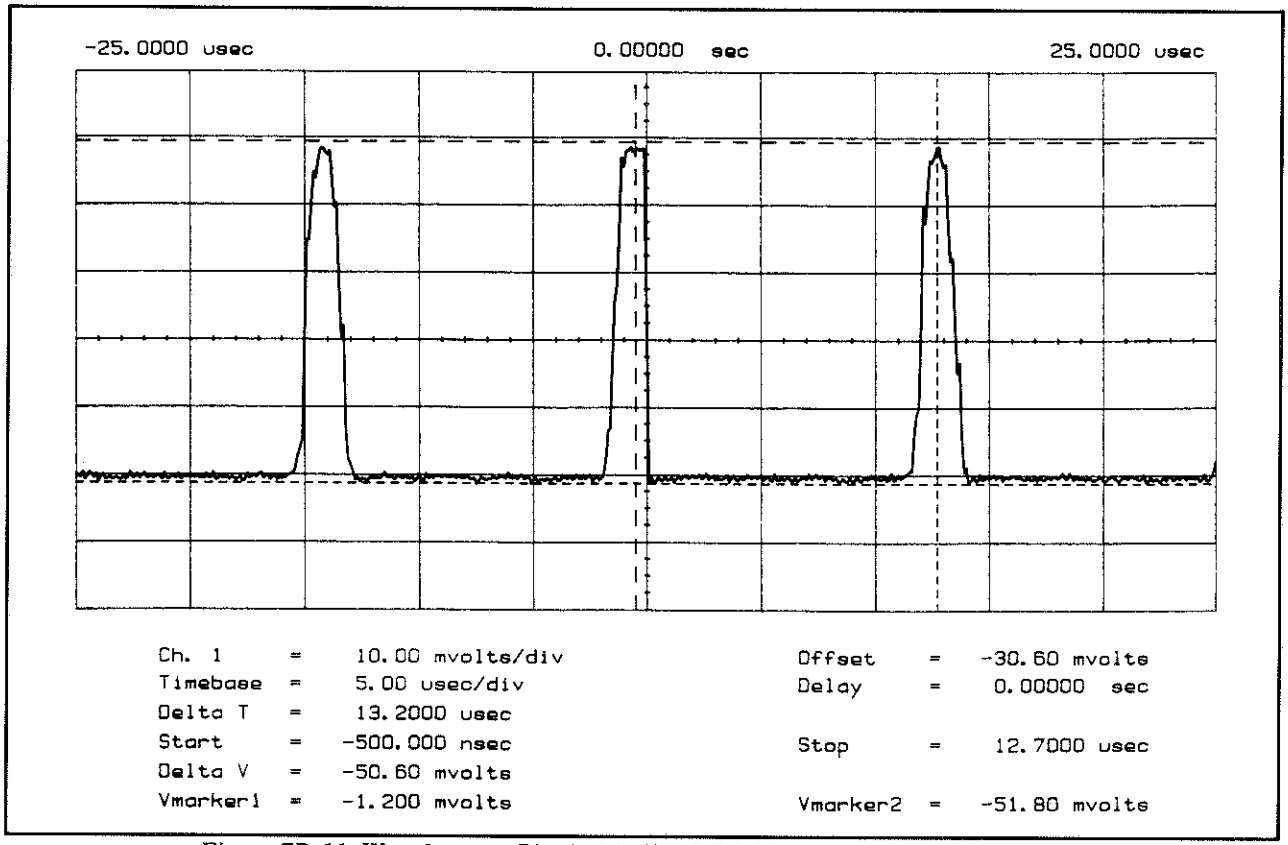


Figure 7D-11. Waveforms at Pin 6 of A4U(4-5,7-8,10,12,14,15,17,21-26,28,31,33)

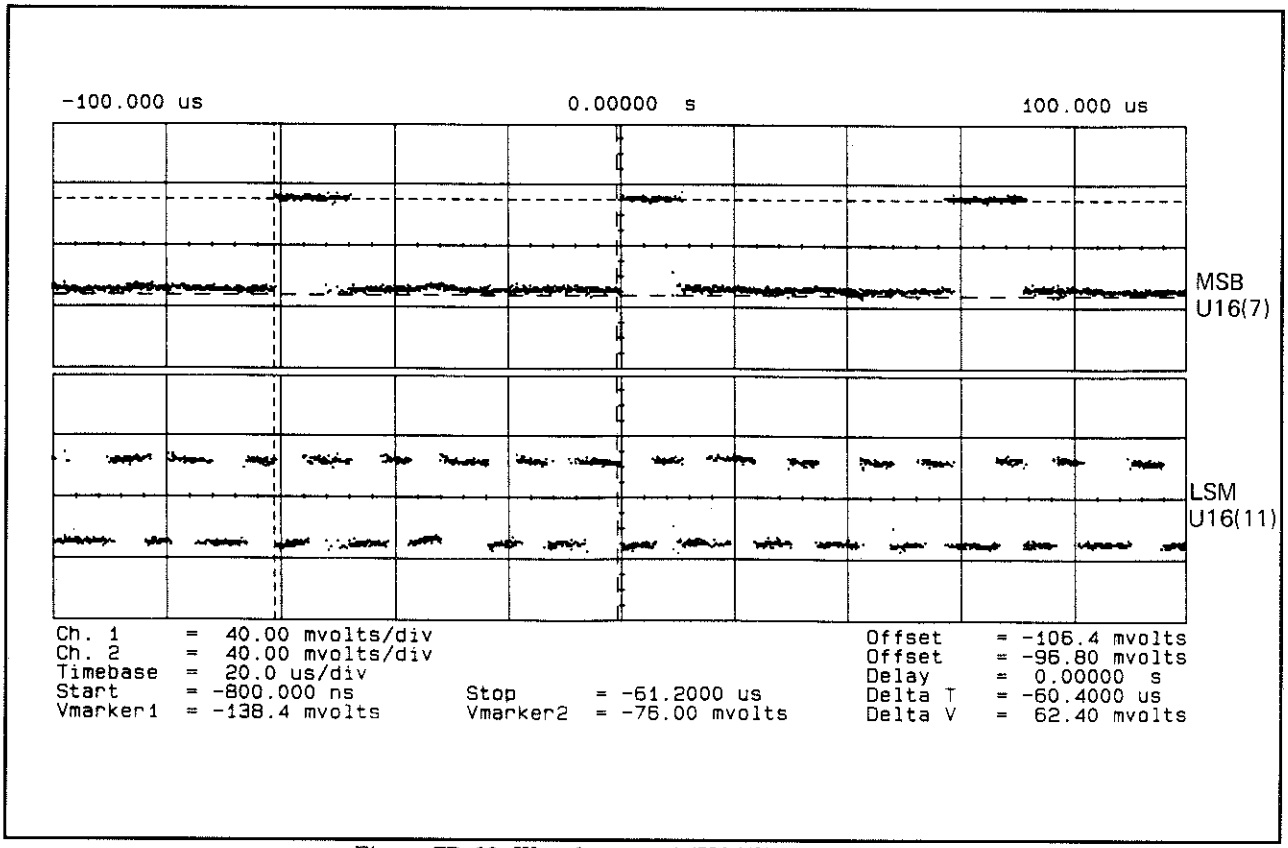


Figure 7D-12. Waveforms at A4U16(3) and A4U27(3)

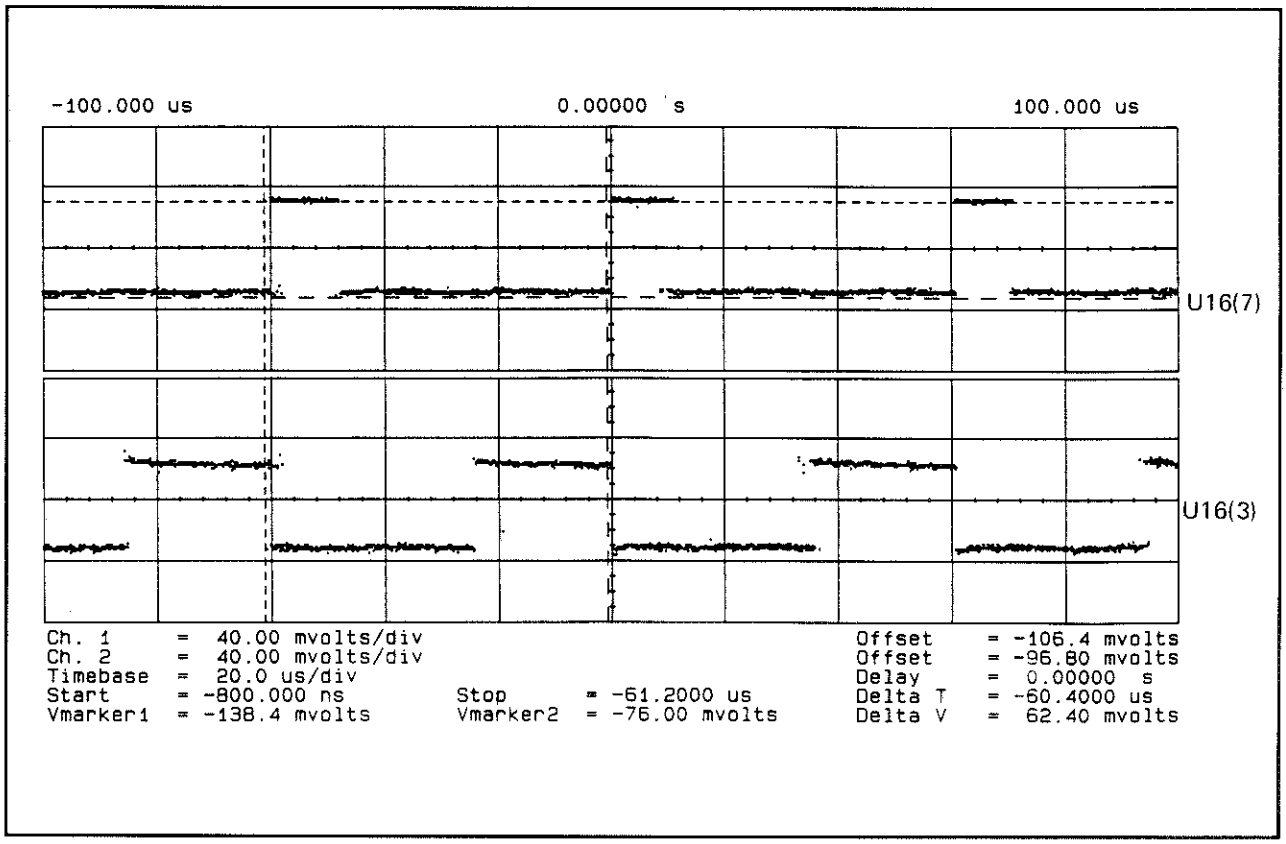


Figure 7D-13. Waveforms at A4U16(7) and A4U27(7)

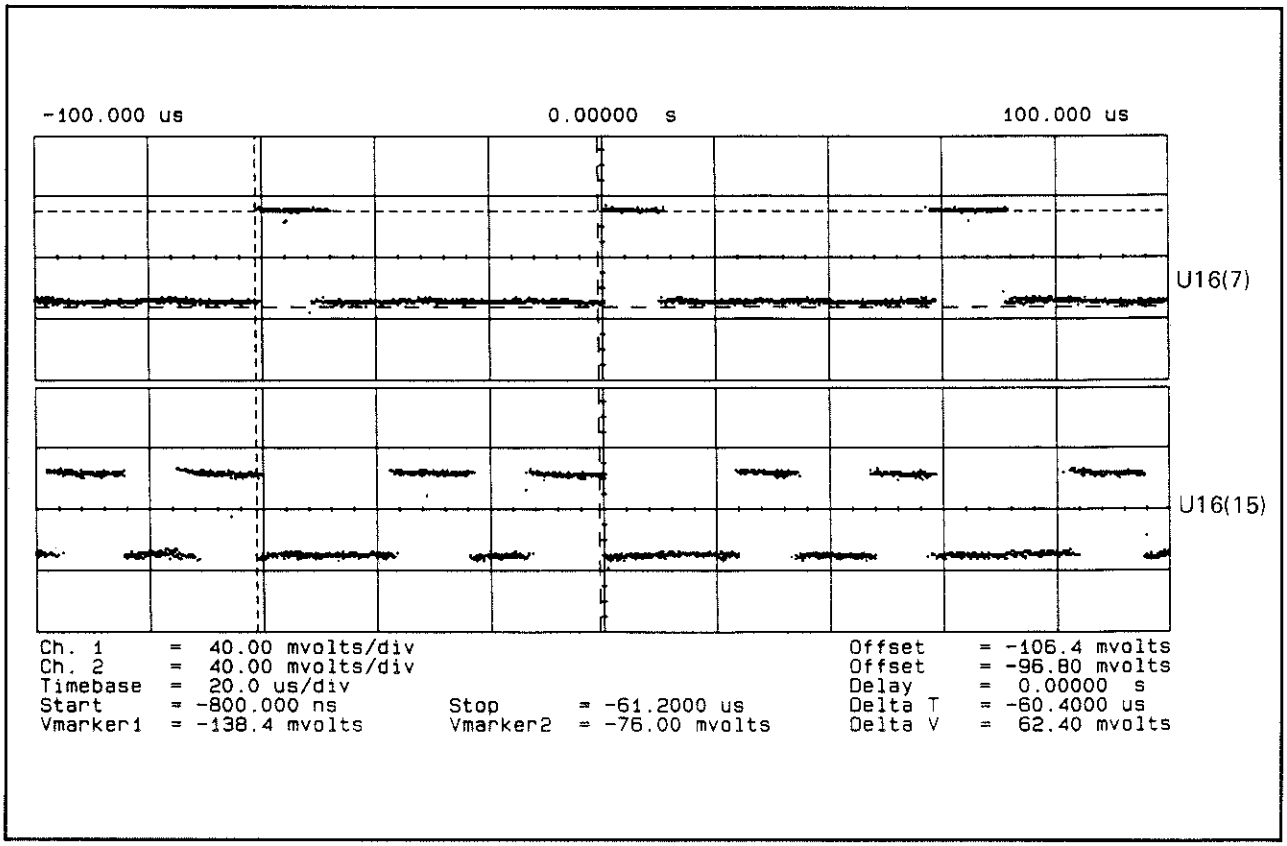
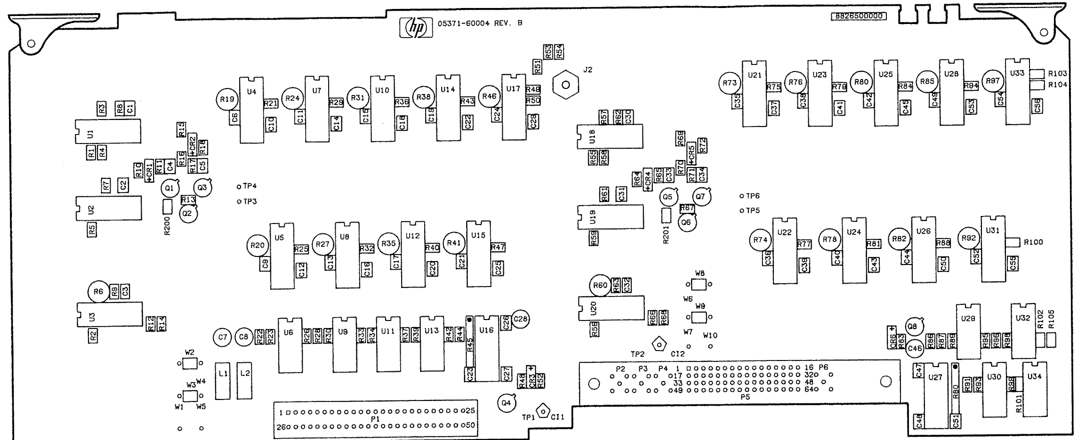
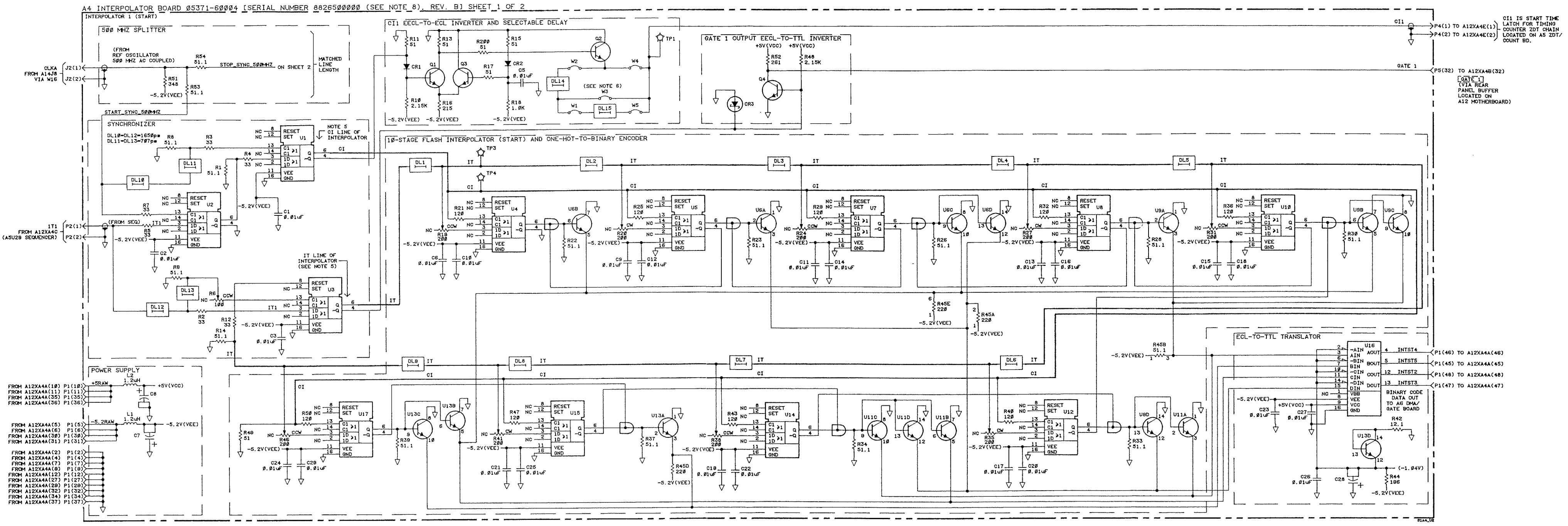


Figure 7D-14. Waveforms at A4U16(11) and A4U27(11)

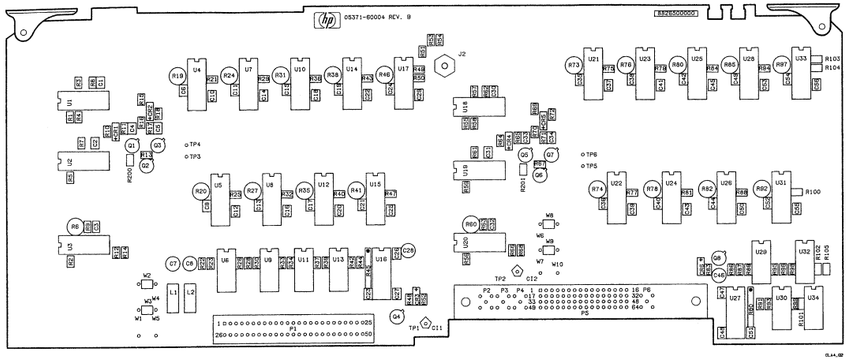




A4 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A4 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. CI AND IT LINES ARE MATCHED LENGTH EXCEPT DL1-DL9 AND DL16-DL24 BOXES REPRESENT ADDITIONAL 200ps OFFSETS.
6. SELECTABLE DELAY LINE FOR "START" INTERPOLATOR (SHEET 1): TYPICALLY ONLY W2 AND W3 ARE LOADED FOR NOMINAL DELAY. A 660ps DELAY MAY BE DELETED BY LOADING ONLY W4 AND A 660ps DELAY MAY BE ADDED BY LOADING ONLY W2, W1 AND W5.
7. SELECTABLE DELAY LINE FOR "STOP" INTERPOLATOR (SHEET 2): TYPICALLY ONLY W8 AND W9 ARE LOADED FOR NOMINAL DELAY. A 660ps DELAY MAY BE DELETED BY LOADING ONLY W6 AND A 660ps DELAY MAY BE INSERTED BY LOADING ONLY W8, W10 AND W7.
8. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

Figure 7D-15. A4 Interpolator Board, Schematic Diagram (Sheet 1 of 2)



A4 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A4 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN MICROHENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. CI AND IT LINES ARE MATCHED LENGTH EXCEPT DL1-DL9 AND DL18-DL24 BOXES REPRESENT ADDITIONAL 200ps OF DELAY.
6. SELECTABLE DELAY LINE FOR "START" INTERPOLATOR (SHEET 1): TYPICALLY ONLY W2 AND W3 ARE LOADED FOR NOMINAL DELAY. A 660ps DELAY MAY BE DELETED BY LOADING ONLY W4 AND A 660ps DELAY MAY BE ADDED BY LOADING ONLY W2,W1 AND W5.
7. SELECTABLE DELAY LINE FOR "STOP" INTERPOLATOR (SHEET 2): TYPICALLY ONLY W8 AND W9 ARE LOADED FOR NOMINAL DELAY. A 660ps DELAY MAY BE DELETED BY LOADING ONLY W8 AND A 660ps DELAY MAY BE INSERTED BY LOADING ONLY W8, W10 AND W7.
8. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE S-01017 PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS, FOR MORE DETAILS. SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

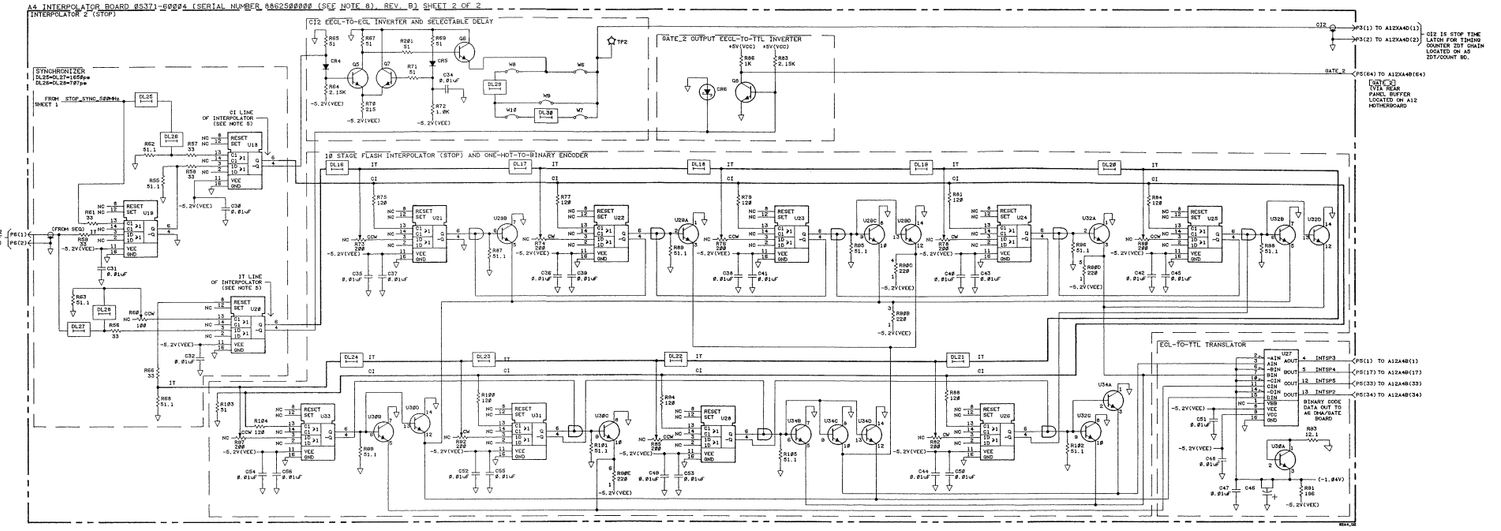


Figure 7D-15. A4 Interpolator Board, Schematic Diagram (Sheet 2 of 2)

7E A5 ZDT/COUNT

SECTION 7E
A5 ZDT/COUNT BOARD

7E-1. Introduction

The A5 ZDT/Count Board performs the following functions:

- makes the continuous count process,
- samples the binary counter without disturbing the count process,
- does the above at reasonable counting rates and data rates with adequate resolution

The two integrated circuits (ICs) that make such a measurement possible are the Sequencer and the six Zero-Dead-Time (ZDT) Counters. The Sequencer directs input signals (measured event clocks), and the arming and gating signals (event latches) to the appropriate ZDT IC and time latches to the A4 Interpolator Board. The ZDT's perform the actual counting of the time or events as specified by the latching signals. The counting results are stored in RAM ICs associated with each ZDT. The measurement information is accessed and sent to either the A7 Processor Board for processing and its subsequent front-panel CRT display, or the A8 I/O Controller Board where the unprocessed binary data is routed through the HP-IB interface circuitry to an external controller for processing.

The functions of the A5 ZDT/Count Board can be summarized as follows:

As specified by the programming of the 68000 μP from the A6 DMA/Gate Board, the Sequencer determines

- When Block Holdoff/Sample Arm conditions (for continuous gating measurements) or Start Arm/Stop Arm conditions (for non-continuous gating measurements) are met,
- When the Start (L11 and L21) and Stop (L12 and L22) latches are sent to their respective Event Counter ZDT chains,
- To which Event Counter ZDT chain CHANNEL A input signal, CHANNEL B input signal, or 500 MHz reference frequency (CLKB) is routed,
- When the first and last measurement edge (IT1 and IT2) are sent to the A4 Interpolator Board for phase comparison with the 500 MHz reference frequency (CLKB). The A4 generates CI1 and CI2 at point of coincidence of the event and clock edges, which trigger the start and stop of the Timing Event Counter, and
- When to send TTR signal to A6 DMA/Gate Board *System Timing Controller* requesting programmed time interval pulses (TG1 or TG2) used during Interval Arming to control when latching of the counter occurs.

As specified by 68000 μP and A6 DMA/Gate Board programming, the Event and Timing Counter ZDT chains perform

- The actual counting of the CHANNEL A and B input signals (events) and the 500 MHz reference frequency (CLKB),
- Temporary storage of measurement count data,
- Generation of Terminal Counts used for edge, event, and time measurement holdoffs or delays, and
- Generation of prescaled counts of input signals on CHANNEL A, CHANNEL B, or the internal 500 MHz reference frequency during Cycle Sampling Mode.

The A5 ZDT/Count Board has five circuit blocks: (1) *Sequencer Hybrid IC*, (2) *Zero-Dead-Time (ZDT) Counter Hybrid IC*, (3) *RAM Write Circuit*, (4) *RAM Address Latches*, and (5) *System Buffers*. The component-level theory of operation for the blocks listed follow. See "A5 ZDT/Count Board Block Diagram" in *Figure 7E-16* for reference.

7E-2. Typical Measurement Cycle

Prior to the start of each measurement cycle, the A7 assembly's 68000 μP programs the Sequencer's arming and gating setup as specified by the user. Meanwhile, the A6 DMA/Gate board programs the A5 *RAM-Write* circuit according to the type of measurement to be made. This circuit generates a series of single pulses for frequency measurements, a series of double pulses for time interval and totalize measurements, and a series of quadruple pulses for totalized time interval measurements.

After setup programming is complete, the 68000 μP automatically initiates the measurement. The Sequencer routes the appropriate inputs to the counting ZDT ICs, while concurrently sending latching pulses to the ZDTs once arming is qualified. When all the measurement latches have been routed to the ZDT, the *RAM Write* circuit generates a pulse train that stores the data at the output of the ZDT to its corresponding RAM. The A6 DMA/Gate Board receives copies of the *RAM Write* circuit pulses for incrementing the RAM Address Counter. When the RAM Address Counter reaches its Terminal Count, TC, signaling the end of the block measurement, a signal RAMTC is sent to stop any further latches from being routed from the Sequencer and RAM-Writing pulses. This signal also serves as an interrupt to the 68000 μP, telling it that the data is now ready for processing.

7E-3. Counting Chain

The counting hardware (*Figure 7E-1*) is comprised of Sequencer A5U29 driving two event-counter chain circuits, and the A4 Interpolator Board. Each event-counter chain consists of two ZDT ICs arranged in cascade increasing overflow detection time. The A4 Interpolator, which makes time-latch resolution of 200 ps, supplies latches to the Timing Counter chain also made up of two ZDT's in cascade. The Timing Counter chain is clocked by the 500 MHz reference signal (CLKB) generated by the A14 Timebase Multiplier Board. When the HP 5371A is not in measurement mode, the Sequencer is reset by SEQ_RS to inhibit its routing any latches to the ZDTs, while the ZDTs themselves are not reset, thus allowing them to be reset.

7E-4. Sequencer IC

The schematic diagram for A5 is shown in *Figure 7E-17*. The Sequencer distributes the latch and clock signals to the ICs that actually perform the counting function, the ZDT's, as prescribed by the specified arming conditions. A simplified block diagram is shown in *Figure 7E-2*. The Sequencer features two-stage sequential arming for both "start-arm" and "stop-arm", external control by terminal count of the selected counting inputs, and a phase comparator for a plus- or minus- time interval measurements. To the 68000 μP, the sequencer appears as a bank of control bit registers that must be programmed for the HP 5371A to perform a desired measurement.

The Sequencer is organized into two almost identical channels, each containing an "arming" and a "clock" section. The "clock" section selects the input from either the CHANNEL A or CHANNEL B to be counted and routes it to the appropriate ZDT clock input. Within the arming section there is a start arm and a stop arm subsection. Each subsection consists a two-stage multiplexer-latch arming structure and synchronizer. When the arming structure qualifies the input signal, the synchronizer is enabled and produces a latch synchronized to the clock output. The "arming" section selects the sources of the latch signals to be sent to the ZDT latch inputs at the appropriate time, after the arming and gating requirements have been satisfied. This section has two similar clock subsections, one for each event ZDT count chain. Once enabled by the "start" arming circuit, each clock subsection is capable of switching clock source upon receipt of the Terminal Count (TC) from the event-count chain.

The Sequencer's main outputs include;

1. L11 (Start Latch), L12 (Stop Latch), and CLK1 (events being counted) for Event Counter 1 chain.

2. L21 (Start Latch), L22 (Stop Latch), and CLK2 (Clock 2) for Event Counter 2.

3. IT1 (Start Latch), IT2 (Stop latch), for Time Counter after comparison with 500 MHz reference frequency on the A4 Interpolator Board.

The count output may be switched in measurement, if the appropriate Terminal count (TC) is asserted. This process allows one ZDT to perform double duty, first as part of the arming circuit and then as a measuring counter.

7E-5. ZDT Counter IC

The ZDT performs the actual counting of time or events within the HP 5371A and outputs the current data or latch-stored data to the A7 Processor's 68000 μP. A simplified block diagram is shown in *Figure 7E-3*.

Current data is output when the counter is in the "infinite" acquisition mode (Measurement size set to 1) while latch-stored data is output (under the control of the A6 DMA/Gate Board) when the counter is in the "block" acquisition mode (Measurement size > 1).

Incoming events or clock pulses are routed to an 8-bit synchronous counter. The MSB of this counter ripples to the input of another 8-bit synchronous counter giving a total counter length of 16 bits. This 16-bit counter synchronizes the latch with the clock signal. The output of the both counter's binary stages are routed to two separately addressable pair of latches totaling 16 bits per pair. Upon receiving a read command from whichever destination requests the read, the 16-bit data word exits the ZDT IC through the chips Input/Output buffers and routes it to either the A7 68000 μP, the A8 DMA/HP-IB circuitry, or into the ZDT's corresponding RAM. If an internal latch command edge is sent to the clock inputs of the ZDT's latches, then the latch clock line goes low, freezing the bit pattern present at the latch input at the instant the latch command became effective. Note that the Sequencer doesn't always produce synchronized latches or the time latch may not be synchronized. To ensure that the latch is synchronized with the clock, the incoming "Latch 1" and "Latch 2" are both synchronized to the incoming clock signal.

The clock output, the 16th (MSB) of the second 8-bit synchronous counter, and the inhibited Latch 1 and Latch 2 signals, are buffered and sent to the second ZDT in the chain, thus allowing extension to 32 bits counter data.

The Terminal Count circuitry of the ZDT detects a state of all logic level "1" in the binary output of the two 8-bit synchronous counters. The TC/P signal line is used to signal the Sequencer when this occurs. The HP 5371A uses the ZDT to signal when some predetermined (preset) time period, or any number "N" of events has occurred. The number "N" can be preset into the counter (ZDT). The ZDT counts up until the Terminal Count (TC) is reached. To generate a TC on a number of events (i.e., measurement input) the Sequencer connects the input channel carrying the events to the ZDT. To generate a time delay, the Sequencer routes the 500 MHz reference frequency (CLK A) to the ZDT. In both cases, the number preset into the ZDT is input 16 bits at a time, and is the number of events or number of clock periods desired. If two cascaded ZDT ICs are preset, the most significant bit ZDT is programmed to propagate down a "TC" true.

7E-6. ZDT and Sequencer Interaction

In the HP 5371A, the ZDT ICs are configured in three chains; each chain having two ZDTs connected in a cascaded manner. Both ZDTs in each chain, ZDT 1 and ZDT 2, each interface with the Sequencer via the CLK, L1, L2, and TC/P lines. The ZDTs in the third chain, the Timing Counter chain, do not interface directly with the Sequencer since its function is to measure time only. The CLK input to this chain is the 500 MHz reference frequency (CLK B) signal, and its L1 and L2 inputs are coincidence output signals, CI1 and CI2, from the A4 Interpolator Board.

For example, consider what happens when the HP 5371A is set up to measure frequency on the CHANNEL A input channel with the measurement gate controlled by CHANNEL B. The Sequencer is programmed to route the CHANNEL A events (input signals) to ZDT1A (A5U22) in the Event Counter 1 chain. The Sequencer also routes the 500 MHz reference frequency to ZDT2A (A5U30) of the Event Counter 2 chain. The rising edge of CHANNEL B input is used internally by the Sequencer to enable the second stage of the two-stage arming circuit. The next event that occurs on CHANNEL A is recognized as the start event and is passed through the enabled second arming stage of the Sequencer and routed as IT1 to the A4 assembly's *Interpolator 1* (Start) interpolator. This ECL-level signal triggers the interpolation process. L11 latches the event count into ZDT1A. When the "Start" interpolator reaches coincidence, the A4 assembly sends the CI1 signal back to the Sequencer, latching the count value (counting the 500 MHz reference frequency) into ZDT2A. This value combines with the value returned from the interpolator to calculate the actual start time of the measurement. The falling edge of the CHANNEL B input enables the second arming stage.

The next event that occurs on CHANNEL A is recognized as the stop event and is passed through the enabled second arming stage. The IT2 signal is now sent to the A4 assembly's *Interpolator 2* (Stop) interpolator. L22 now latches the event count into the ZDT 2A. When the "Stop" interpolator reaches coincidence, it sends the CI2 signal to the Sequencer latching the value of the ZDT counting the 500 MHz reference frequency. This value is combined with the value returned from the "Stop" interpolator to compute the actual stop time. The A7 assembly's 68000 μP can now compute the unknown frequency on CHANNEL A using the count and time values returned from the ZDT's and interpolators.

As another example, consider configuring the HP 5371A to make a Time Interval measurement between the "mth" and "nth" events on CHANNEL A input following a trigger signal from the EXTERNAL ARM input. This measurement is implemented using Event Counter 1 and Event Counter 2 ZDTs and illustrates the Sequencer's flexibility by switching input signals to a ZDT during a measurement. Event Counter 1 ZDT will count "m" events on CHANNEL A and then switch to counting the 500 MHz reference frequency. Concurrently, the Event Counter 2 ZDT will count "n" events. The process begins when the 68000 μP resets the Sequencer thereby blocking both clock outputs to Event Counter 1 and Event Counter 2 ZDTs. Then, Event Counter 1 ZDT is preset to the value that will generate a Terminal Count after "m" events have occurred. In a similar fashion, Event Counter 2 ZDT is preset to generate a Terminal Count after "n" events have occurred. The Sequencer is programmed to use either the CHANNEL A input or the 500 MHz reference frequency as the ZDT clock during this particular measurement setup. When the TC/P1 line is false, the CHANNEL A input is selected. Conversely, when TC/P1 is true, 500 MHz reference is used as the ZDT clock. When the external trigger (EXTERNAL ARM) arrives, clocks to both ZDTs are enabled simultaneously. Both ZDTs begin counting events input on CHANNEL A. After "m" events have been counted, the TC/P1 goes true. This sends IT1 to the A4 "Start" interpolator and switches so that Event Counter 1 ZDT receives the 500 MHz reference instead of the CHANNEL A input. This switching process always finishes before the interpolator reaches coincidence. When the "Start" interpolator reaches coincidence, CT1 is returned to the Sequencer enabling the L11 signal output. After "n" events have occurred, the TC/P2 goes true and sends IT2 to the A4 "Stop" interpolator.

The ZDTs are also capable of being preset and counting a known frequency for the purpose of generating an accurate time delay. Having a 500 MHz reference frequency gives a 2 nanosecond resolution.

7E-7. RAM Write Circuit

The *RAM Write* circuit generates a series of write pulses used for storing ZDT measurement data in RAM, changes the ZDT address so that the ZDTs can alternate the output of two-latch data, resets the Sequencer and the ZDTs at the end of each measurement cycle, and prevents (holds off) the execution of the last write pulse at the end of a block of measurements until told to do so by the 68000 μP.

7E-8. LATCH AND DMA CLOCK SYNCHRONIZATION AND CAPTURE

AND gate A5U14A detects the completion of measurement latching by ANDing signals L11 and L12. A high at A5U14A output, WR_START, starts the RAM Write circuit. Gate A5U7A synchronizes the write start signal, WR_START, to the 125 MHz DMACLK. A5U7A also stretches the write start signal until the measurement is complete (i.e., if a measurement requires two latches, the WR_START remains high until the second write is complete). This is accomplished by routing output high to common clock disable (pin 9 of A5U7B) which stretches the start write signal until A5U7A is reset at the end of the measurement. AND gate A6U8A allows counter A5U12 to reload and restart the RAM Write circuit. For measurements that require more than one write pulse, the counter must reload and restart until the required number of write pulses have been generated. A5U8A uses the counter's own terminal count output (pin 4 of A5U12) and the detection of both latch signals to reload and restart the counter. When the terminal count switches low, the counter reloads. After loading is complete, the terminal count output switches high, which enables the counter to start.

7E-9. STATE MACHINE (MASTER CONTROL)

A5U12 is an ECL, 4-bit counter with synchronous load clocked by the 125 MHz DMACLK line whose outputs are decoded to generate the measurement RAM write pulses, Sequencer and ZDT reset signals, and DMA address counter

write pulse, WR_TO_DMA. To maximize the DMA rate, the counter is preset to eight. The counter reloads the counter's preset value when the preset pin 12 is set low. Setting pin 12 high, initiates the counting process.

7E-10. STATE DECODER

The *State Decoder*, which is comprised of AND gates A5U8BCD, decodes the output of counter A5U12 and generates the event and time RAM WR pulses (required to store latched event data in the measurement RAMs), the Sequencer and ZDT reset signals (ZDT_RS(EVT), ZDT_RS(TIM), and SEQ_RS), and resets latch A5U7A. XOR gate A5U102 output goes low 16 ns before the end of the write cycle and goes on again at the end of the write cycle. The output of A5U102 is wire-ORed with the 68000 μP write pulse, UP_ECL. UP_ECL permits the microprocessor to control writing data to the measurement RAMs. By formatting the data, the microprocessor is informed when measurement data is on the data bus and when a data word begins and ends.

7E-11. 1, 2, 4 LATCH DIVIDER

The *1, 2, 4 Latch Divider* generates a gating signal which resets the Sequencer and ZDT ICs at the end of each measurement. Also, signal ZDT_ADDRESS is generated allowing ZDT address bit 0 to change without 68000 μP's intervention. This permits the alternate reading of Latch 1 (L11 and L21) and Latch 2 (L12 and L22) measurement and interpolator data from measurement and interpolator RAM. Control signals BS • ~T and BS+~T, both generated by the A6 DMA/Gate Board, are decoded by this circuit block to determine whether the measurement will be a single-write, double-write, or quadruple- write measurement. The two control signals are decoded as follows:

	Write Mode		
Control Signal	Single	Double	Quadruple
BS*~T	logic "high"	logic "low"	logic "low"
BS+~T	logic "high"	logic "low"	logic "low"

Figures 7E-4 through *7E-6* show the timing diagrams for single, double, and quadruple measurements.

For a measurement requiring a single-write pulse, gating signal ~GATE_RS is set low continuously allowing the generation of a reset after each write cycle. A double-write measurement sets ~GATE_RS low only during the second write cycle, preventing reset at the end of the first write. Signal ZDT_ADDRESS toggles from reading Latch 1 during the first write to reading L2 during the second write. For a quadruple-write measurement, gating signal ~GATE_RS is low only during the fourth write. ZDT_ADDRESS toggles at the end of the second write.

RS flip-flop A5U4A is configured as a divide-by-two counter. The *State Decoder* provides a rising edge clock at the end of each write. In the single-write mode, A6U4A is set all the time. In other write modes, the flip-flop will toggle. AND gate A5U14B output is wire-ORed with signal SINGLE_ECL. The state of the wire-OR output, signal ZDT_ADDRESS, is determined by the type of measurement being made.

- Single-write measurements — ZDT_ADDRESS is logic "high".
- Double-write measurements — ZDT_ADDRESS toggles from logic "high" to logic "low" at the end of the first write.
- Quadruple-write measurements — ZDT_ADDRESS toggles from logic "high" to logic "low" at the end of the second write.

A5U4B is also configured as a divide-by-two counter. A5U4A provides the clock input to A5U4B. This flip-flop remains in the reset state in single- and double-write measurements. The flip-flop toggles when in quadruple-write mode. At the beginning of each block of measurements, both flip-flops are set by applying a logic "high" via the SYSIN line. A5U14D decodes A5U4AB outputs generating the gating signal for the Sequencer and ZDT IC resets. Pin 15 of A5U14D is high only during the last write pulse of the measurement so that the resets are gated during the

last write. During single-write measurements, pin 15 is always high. OR gate A5U9C ORs ~ZDT_GATE_RS with MASTER_RS so that *Initialization* block reset can inhibit the starting of counter A5U12 via latch A5U7A. The master reset signal is active ("high") when the HP 5371A is not making a measurement. A5U14C gates the SEQ_RS_HOLD with gating signal GATE_RS generating SEQ_GATE_RS. A5U9A ORs SEQ_GATE_RS with the MASTER_RS signal preventing the Sequencer from sending latches to the ZDT counters when the HP 5371A is not in measurement mode.

7E-12. INITIALIZATION CIRCUIT

This circuit inhibits RAM WR pulse generation at the end of each measurement by halting the *State Machine* counter and resetting the *Sequencer* IC. This process effectively stops the counting hardware and allows the HP 5371A to process the measurement data. At the end of the last write pulse, the *Sequencer* must be reset to prevent its sending any more latches to the ZDT counter ICs. The ZDTs do not reset at this time allowing the 68000 μP and A6 DMA/Gate Board to program them for the next measurement. Flip-flop A5U7B detects the last measurement by monitoring the A6 assembly's *DMA Address Generation* counter terminal count signal, RAMTC. Since the address counter is programmed one count ahead of the latched outputs, RAMTC will go high after the second to last write. Therefore, when flip-flop A5U7B detects RAMTC high, the last write pulse from *State Decoder* gate A5U8D (pin 9) will set the MASTER_RS line high. Having the *Initialization* block set high keeps the *Sequencer* in reset mode and hold the RAM_WR lines high (or inactive). For instance, assume a measurement requires ten measurement RAM storage locations. The ZDT counter should write to ten RAM locations ONLY. The *Initialization* circuit holds the RAM WR lines high after the tenth write pulse.

7E-13. SEQUENCER RESET HOLDOFF

Flip-flop A5U100A prevents resetting of the *Sequencer* IC until after the current measurement is complete and the event ZDT ICs have reset. The output of A5U100A, SEQ_RS_HOLD, controls the gating of the *Sequencer* reset signal through AND gate A5U14C. Data is clocked into the flip-flop by a delayed version of the event counter reset signal, ZDT_RS(EVT). The flip-flop is set after detection of both latch signals L11 and L12. The flip-flop is reset by clocking in a MASTER_RS low after the ZDTs have been reset. Recall that MASTER_RS is low while a measurement is in progress.

7E-14. RAM Address Latches

The *RAM Address Latches* latch the measurement RAM addresses generated by the A6 DMA/Gate Board's *DMA Address Generation* circuit to the A5 ZDT/Count Board's DI/O00-DI/O15 data bus lines. Latches A5U1 and A5U5 provide addresses for the twelve measurement RAMs located on the A5 ZDT/Count Board. Gate delays introduced by the A6 DMA/Gate and A5 ZDT/Count Board's circuitry are offset by using the current write pulse (N) to generate the NEXT measurement RAM address and to latch the current address generated by the last write pulse (N-1) to the measurement RAMs. This is why the latched address at A5U1 and U5 always represents the measurement RAM address for next write cycle.

7E-15. System Buffers

The bidirectional *System Buffers* A5U43 and A5U47 connect the ZDT/Gate board's DI/O00-DI/015 data bus lines to the Count Hardware Data Bus (CTD0-CTD15). The direction of data flow through the buffers is controlled by the 68000 μP's count read/write signal CTRW. When CTRW is logic high, the buffers allow the ZDT/Count board to pass data from its own data bus to the Count Hardware Data Bus. When CTRW is logic low, the buffers allow data to pass from the Count Hardware Data Bus to the ZDT/Count board's data bus. The A6 DMA/Gate Board's *PAL Decode* IC A6U36(pin 12) DATAEN signal controls both buffer enable lines. DATAEN is at logic low during all data transfers. Setting DATAEN to a logic high, isolates the Count Hardware Data Bus from the ZDT/Count board's data bus.

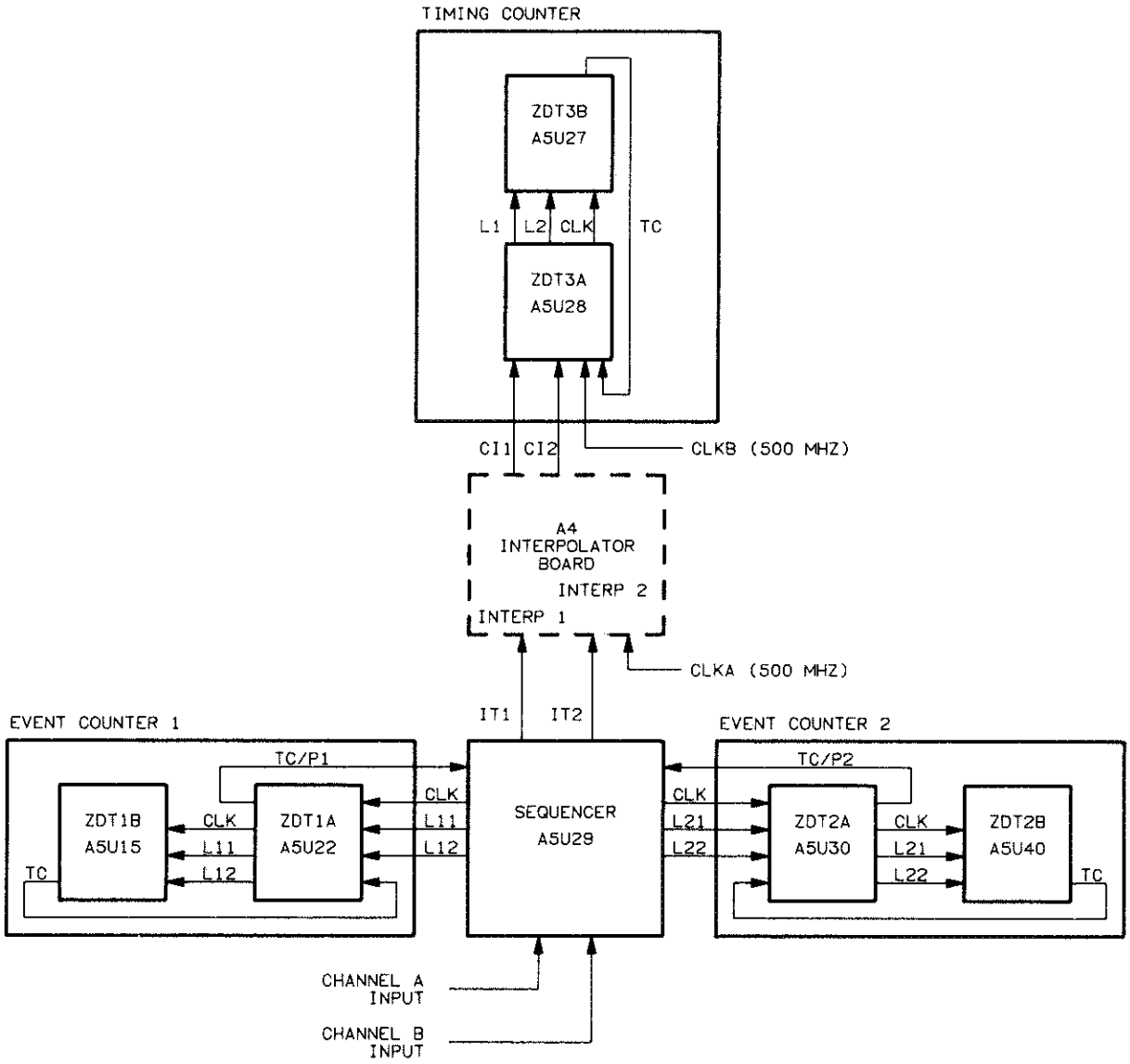


Figure 7E-1. Counting Chains

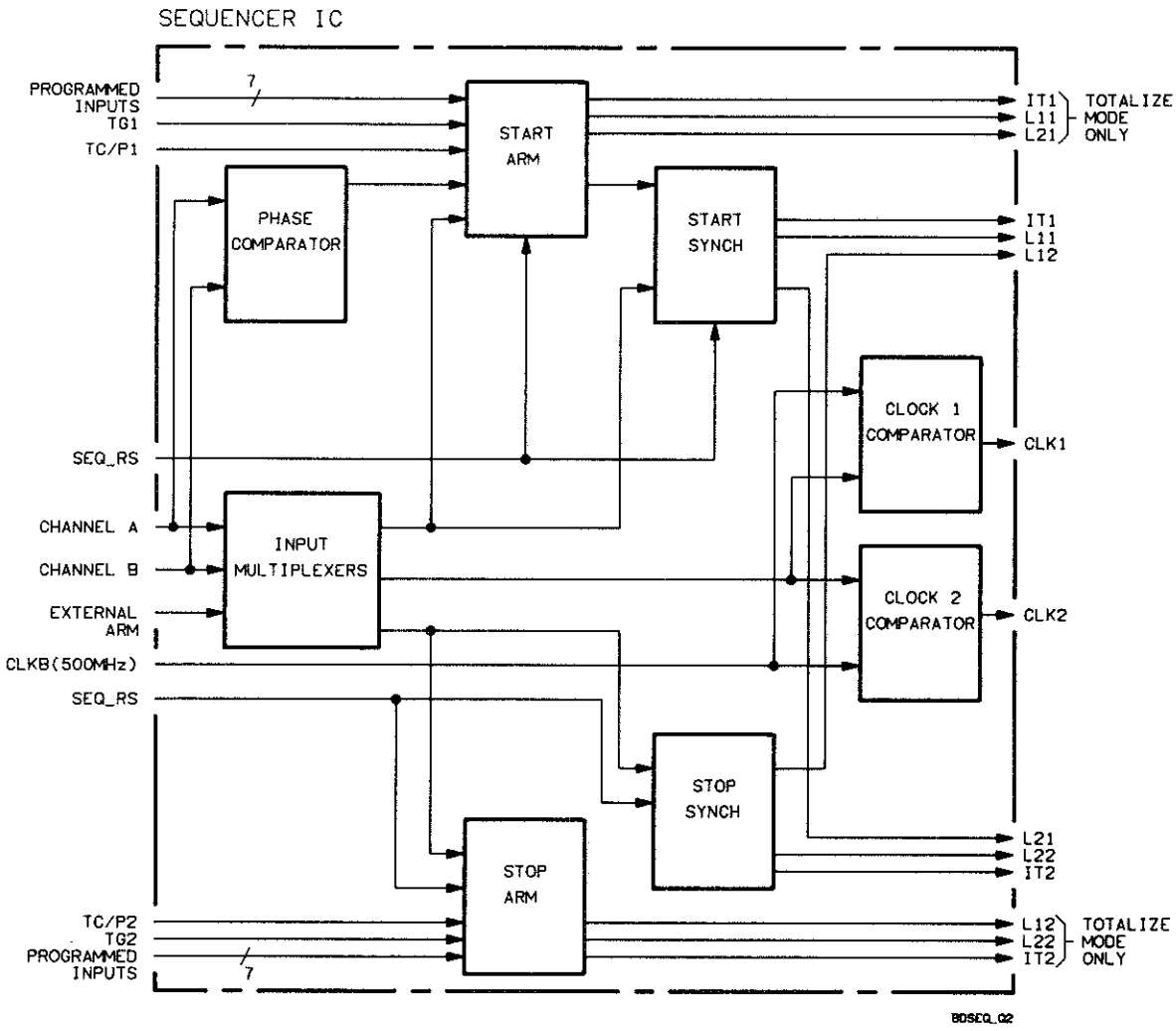


Figure 7E-2. Simplified Sequencer IC Block Diagram

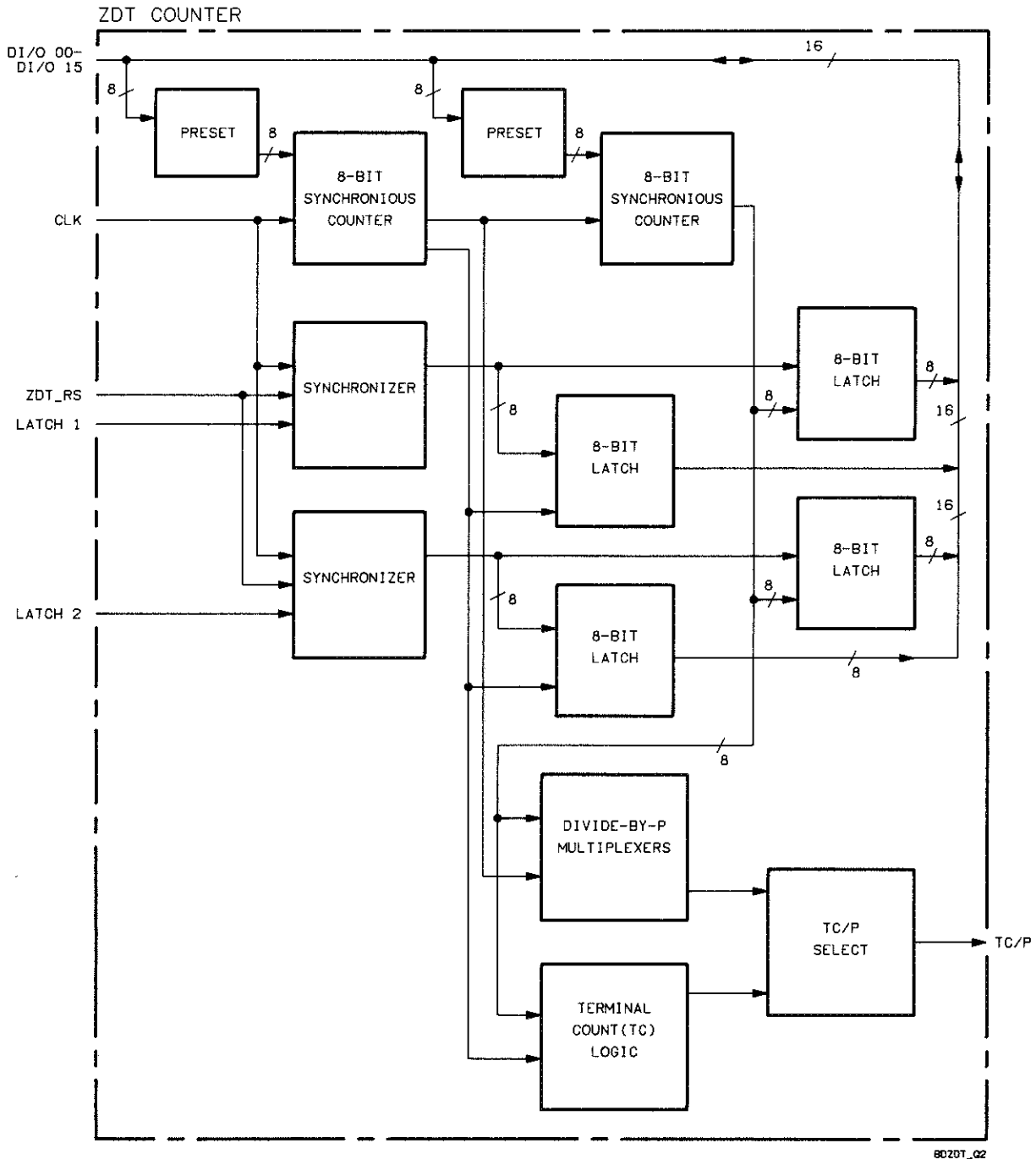


Figure 7E-3. Simplified Zero-Dead-Time (ZDT) Counter Block Diagram

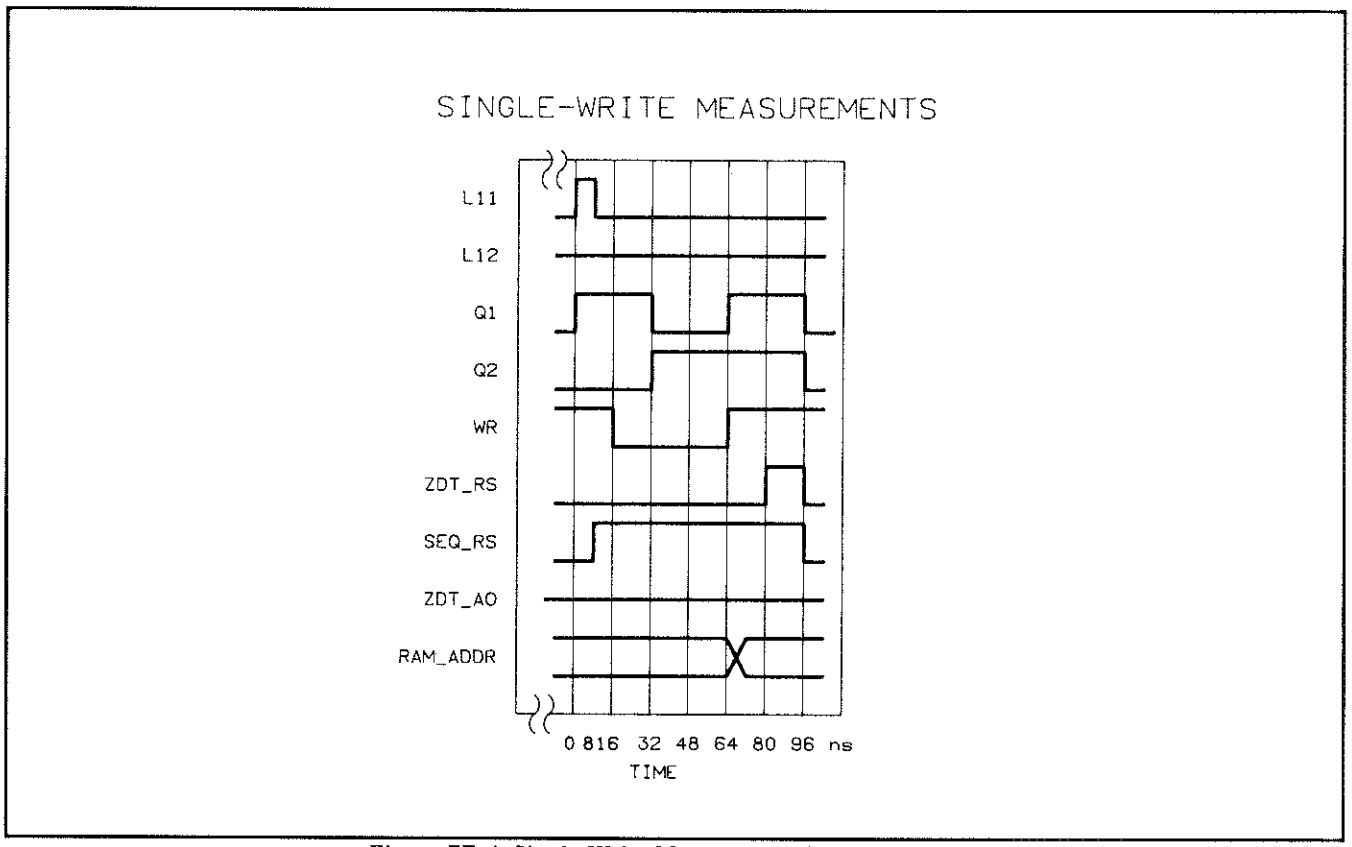


Figure 7E-4. Single-Write Measurement Timing Diagram

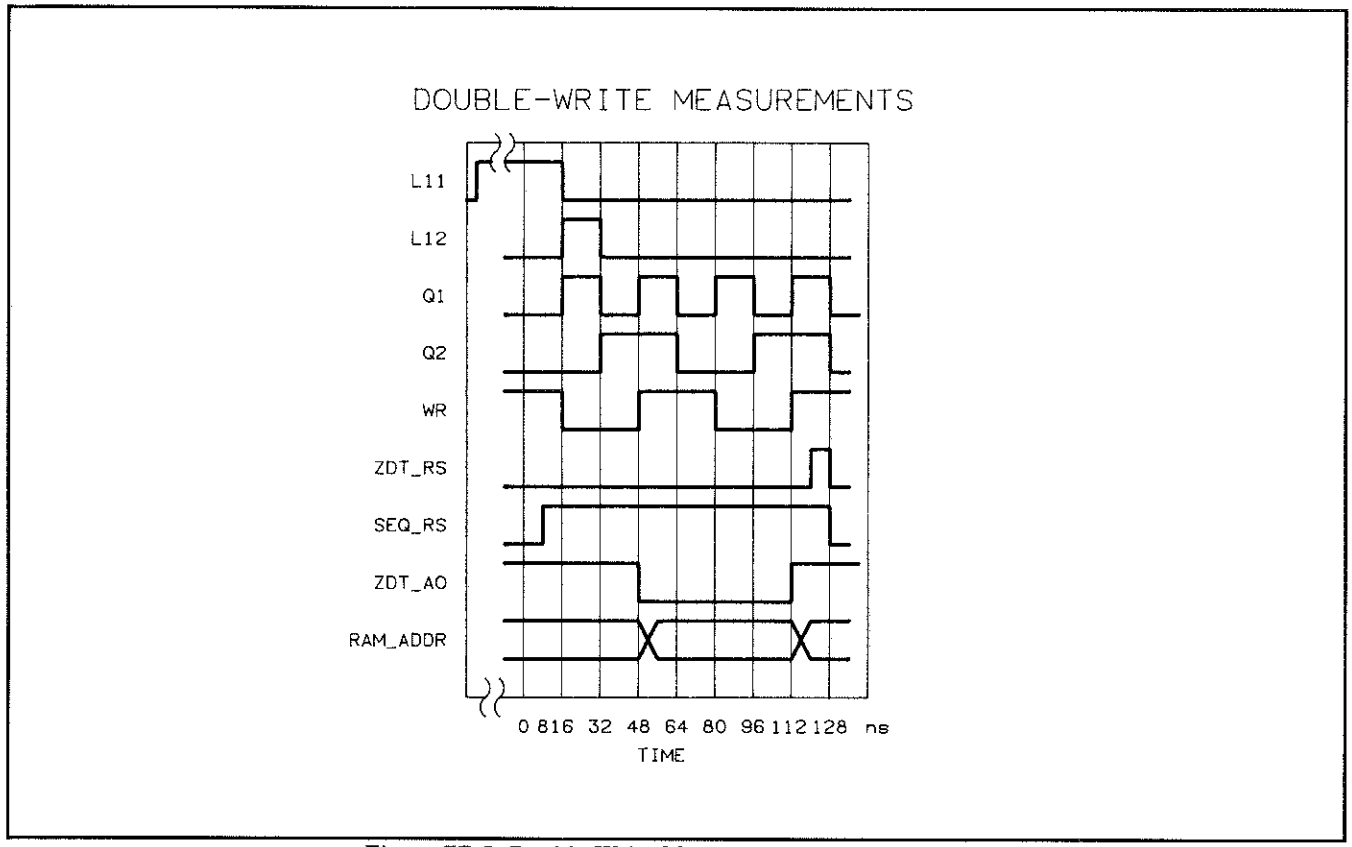


Figure 7E-5. Double-Write Measurement Timing Diagram

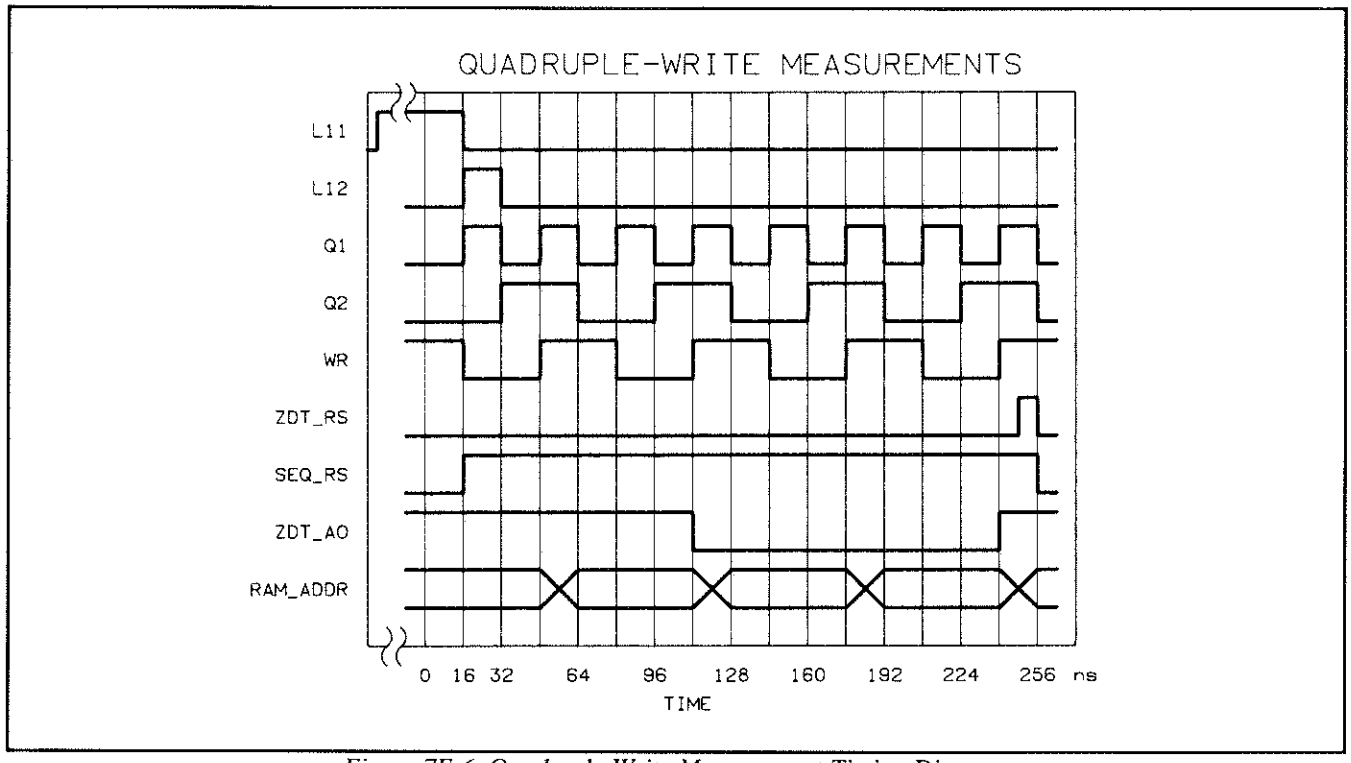


Figure 7E-6. Quadruple-Write Measurement Timing Diagram

7E-16. A5 ZDT/Count Board Troubleshooting

7E-17. TEST EQUIPMENT REQUIRED

- HP 1725A Oscilloscope
- HP 3325 Function Generator
- A20 Count Extender Board (HP Part Number 05371-60017)
- DMA Extender Cable (HP Part Number 05371-60225)

7E-18. DIAGNOSTICS

- Diagnostic Test 5. "Count ICs"
- Diagnostic Test 7. "Measurement RAM"

7E-19. BACKGROUND

The A5 ZDT/Count board contains the hardware that counts and stores the input signal pulses (or events). The A5 assembly consists of the six following circuit blocks:

- Sequencer
- RAM Write Circuitry
- Measurement RAM Circuitry
- Event Counter 1 Chain
- Event Counter 2 Chain
- Timing Counter Chain

The Event Counter and Timing Counter chains are identical circuits. The Event Counter ZDTs (Zero-Dead-Time) count input events while the Timing Counter ZDTs count 2 ns periods. Each chain includes two ZDT Counters, four Measurement RAMs, and four Internal Bus Buffers. The Sequencer IC and the six ZDTs make the "continuous" count process possible. There is a total of twelve Measurement RAM ICs, four per chain. Also included in the Measurement RAM circuit are two data bus buffers and two RAM address latches.

Following are definitions of the various logic levels used in the troubleshooting procedure.

	EECL	ECL	TTL
Logic 1	0 V	–0.8 V	5 V
Logic 0	–0.5 V	–1.7 V	0 V

7E-20. A5 TROUBLESHOOTING PREPARATION

A. Place the A5 assembly on the A17 Count extender board. Leave the DMA cable from the A6 Board unattached.

B. Connect the external frequency output (10 MHz) from the rear panel to Channel A input at the front panel.

C. Set the HP 5371A to measure Frequency in the Automatic arming mode.

7E-21. A5 TROUBLESHOOTING PROCEDURE

7E-22. RAM Write Circuit and Sequencer

The first step in troubleshooting is to check the RAM Write Circuit. During the procedure, refer to sheet 1 and 2 of the A5 schematic.

NOTE

In a continuous measurement, LATCH11 and LATCH12, represent the holdoff and sampling signals. In the automatic mode where no holdoff is used, LATCH11 is low or inactive. However, LATCH12 toggles at a frequency exactly the same as that of the input signal, which in this case is the 10 MHz reference clock signal.

Internally, the two LATCH signals transform into the Count/Load signal of the State Machine, which is a 4-bit counter. If the LATCH signals are present and the RAM_WR signal is still absent, then suspect that the trouble lies in either the STATE MACHINE, the STATE DECODER, or the ECL-TTL TRANSLATOR.

In step D, the STATE MACHINE is checked first by verifying the clock signal, the Count/Load signal, and the second least significant bit of the counter. Since the clock speed of the counter is 125 MHz and the Count/Load signal toggles (due to the fact that LATCH12 toggles at 10 MHz), expect to see the 2nd least significant bit toggle every 16 ns (2 * clock period) when the Count/Load signal is high, and remains high when the count/load signal is low.

D. Observe the RAM_WR (TIM) signal at A5U31(27). If the signal is a 10 MHz square wave with Vmax greater than 2.4 V and Vmin less than 0.4 V, then the RAM Write Circuit is functioning properly. An example of the signal is shown in *Figure 7E-7* below:

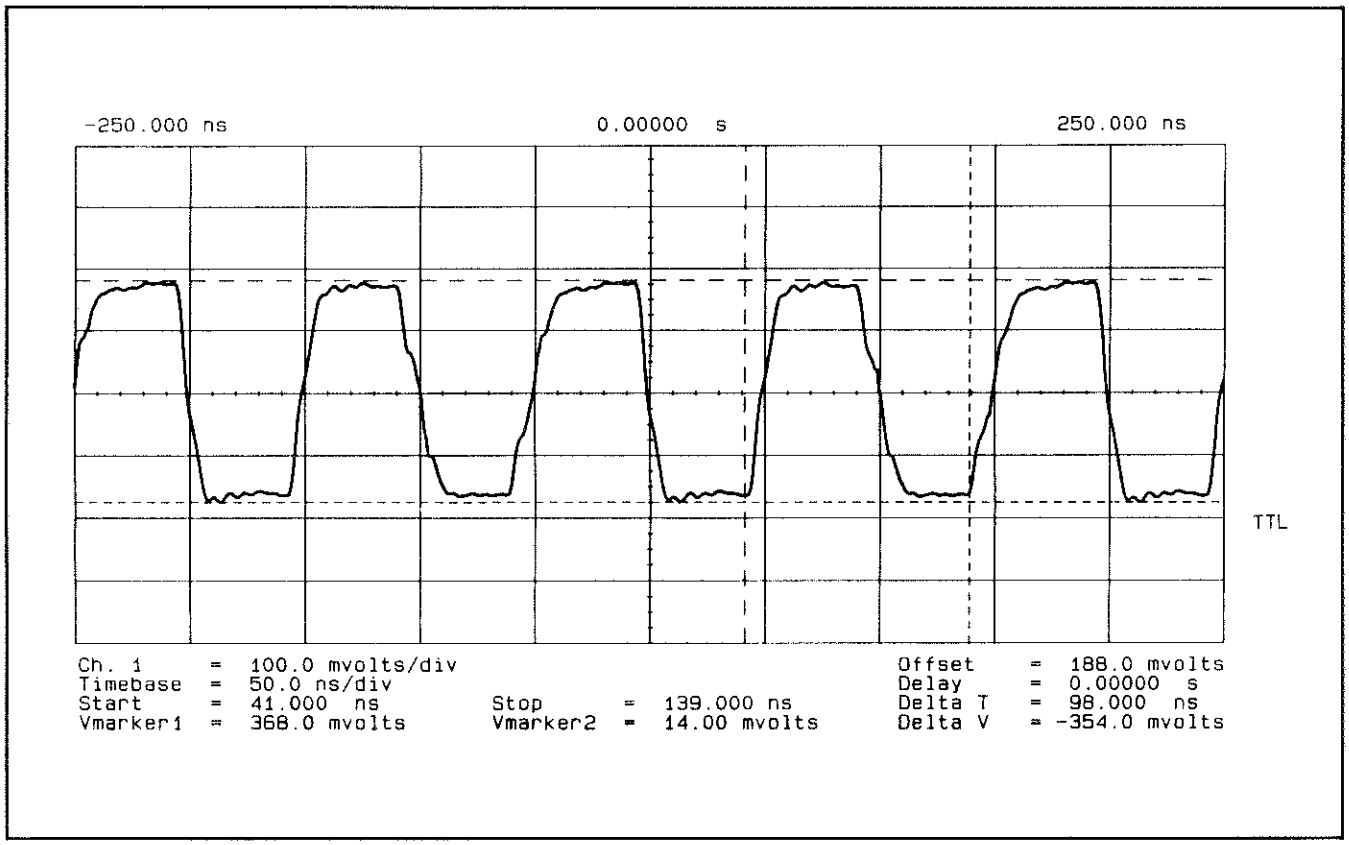


Figure 7E-7. RAM_WR (TIM) Signal at A5U31(27)

E. If the RAM_WR signal is not present as indicated above, check LATCH11 at A5U14(4) and LATCH12 at A5U14(5). Observe that LATCH11 is low (ECL level) and that LATCH12 is a 10 MHz signal (ECL level) as shown in *Figure 7E-8.*

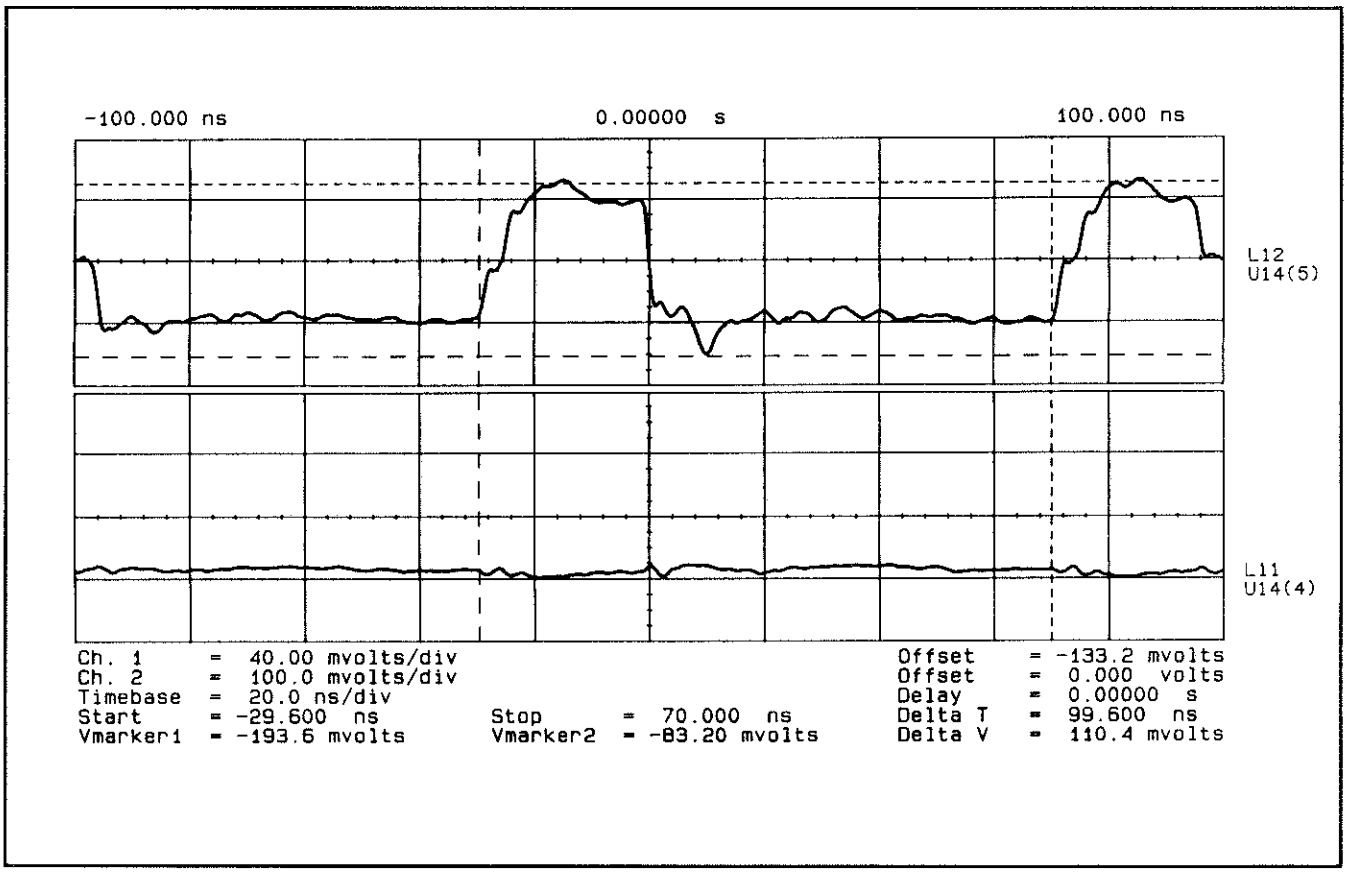


Figure 7E-8. Latch 11 and Latch 12

F. If LATCH11 and LATCH12 are not similar to the waveform shown above, then the Sequencer (A5U29) is malfunctioning. Go to the Sequencer Troubleshooting Procedure.

G. If LATCH11 and LATCH12 signals are correct but the RAM_WR is not, then perform the following:

1. Check the 125 MHz signal at A5U12(13). An absence of the signal indicates that the A14 board is not generating the clock signal for the State Machine. In this event, troubleshoot the A14 board.

2. If the clock signal is present, then check the State Machine, which is a 4-bit ECL counter (A5U12). Probe A5U12(2) and verify that the signal is similar to that in the *Figure 7E-9.*

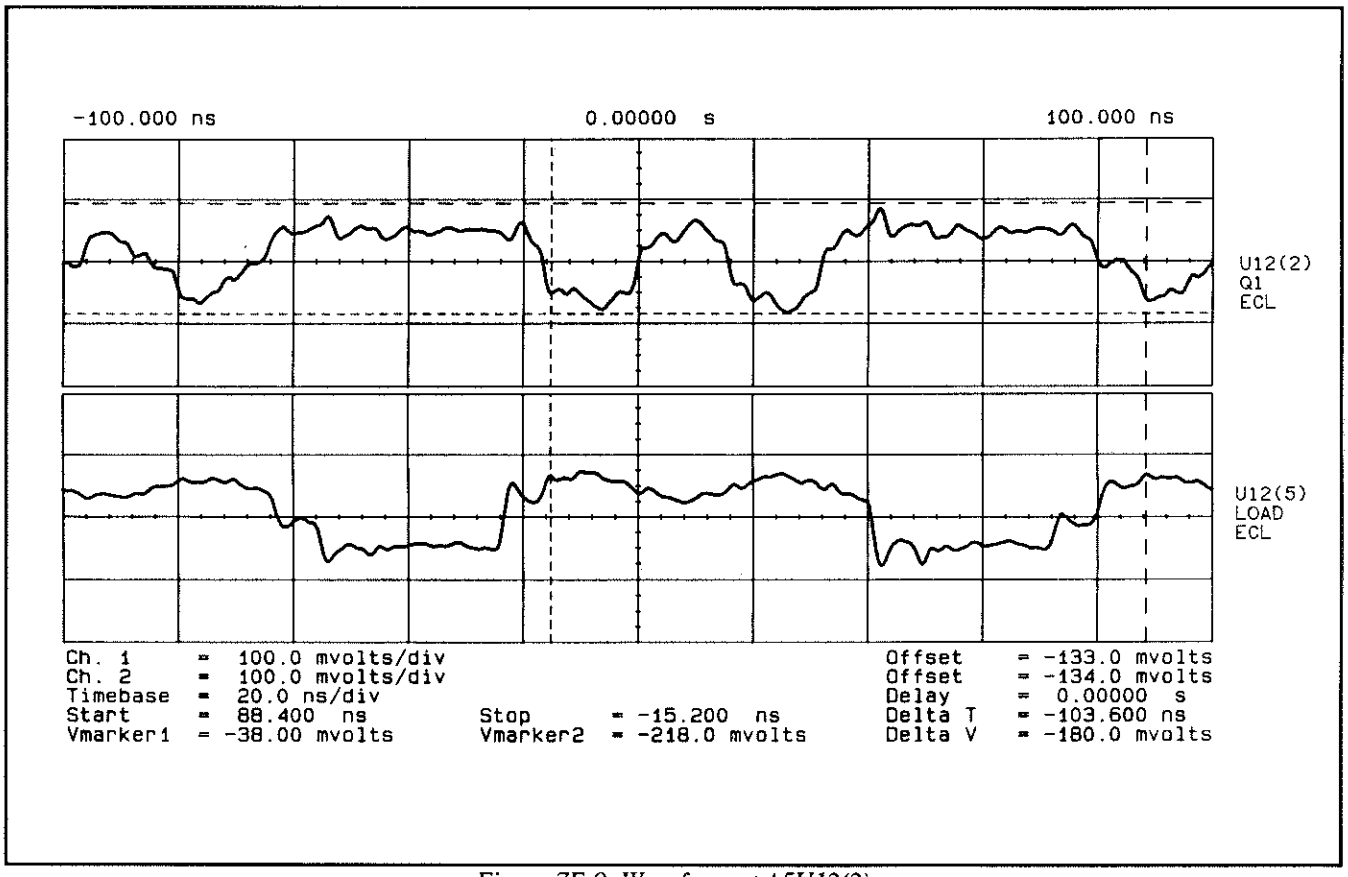


Figure 7E-9. Waveform at A5U12(2)

3. If the output at A5U12(2) is correct, then the trouble lies in either the State Decoder (A5U8) or the ECL-TTL Translators (A5U2 and A5U11). Check the ECL-TTL Translators by verifying that A5U2(2), the input of the translator, is a 50% square wave with a period of 100 ns at an ECL level. If correct and the output, the RAM_WRITE signal, which was checked earlier, is incorrect, then the translator is at fault. Replace the ECL-TTL decoders, U2 and U11. However, if the input is incorrect as well, replace A7U8.

4. If the output at A5U12(2) is incorrect, then verify that A5U12(5) has a period of 100 ns with a waveform similar to that shown in *Figure 7E-10* below:

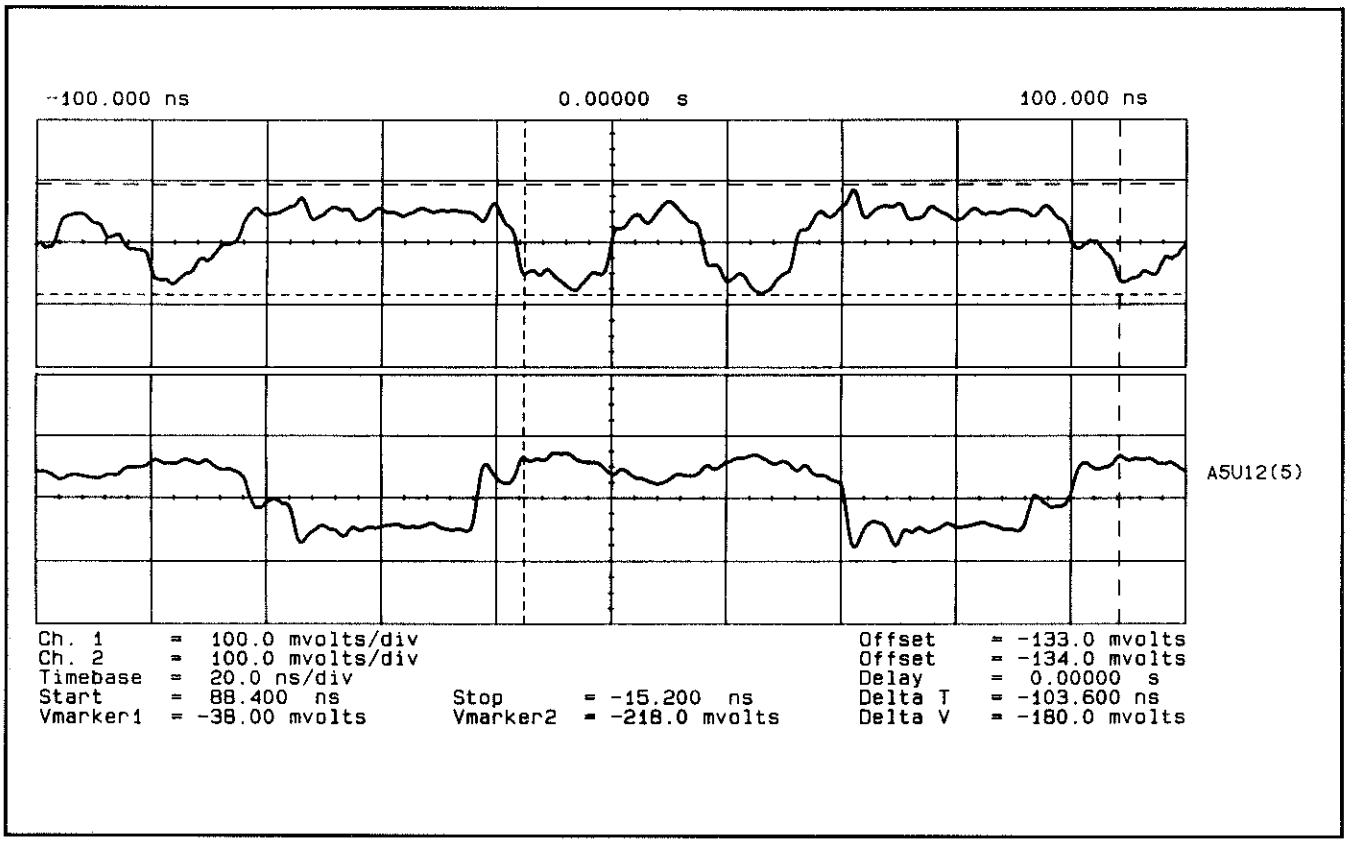


Figure 7E-10. Waveform at A5U12(5)

5. Change A5U12 if the signal is correct. However, if the signal is incorrect then the trouble lies to the left of the schematic for the State Machine. In this case, change U3, U8, U14 and U7. If the trouble persists, then the error most likely comes from the A6 DMA/Gate Board PAL which helps generate the ~UPWR signal to A5U3.

7E-23. Sequencer

NOTE

Two important signals that affect the SEQUENCER's ability to generate the LATCH11 and the LATCH12 signals are the input signal, A5U29(A4), and the SEQ_RS signal, A5U29(C11). Upon receiving the input signal and the SEQ_RS which is generated by the 1,2,4 LATCH DIVIDER, the SEQUENCER generates the appropriate LATCH signals. The 1,2,4 LATCH DIVIDER generates the SEQ_RS signal at a certain frequency depending on the type of measurement being made.

A. Verify that a 10 MHz signal is present at the Channel A input of the Sequencer, A5U29(A4), and at SEQ_RS, A5U29(C11). See *Figure 7E-11*.

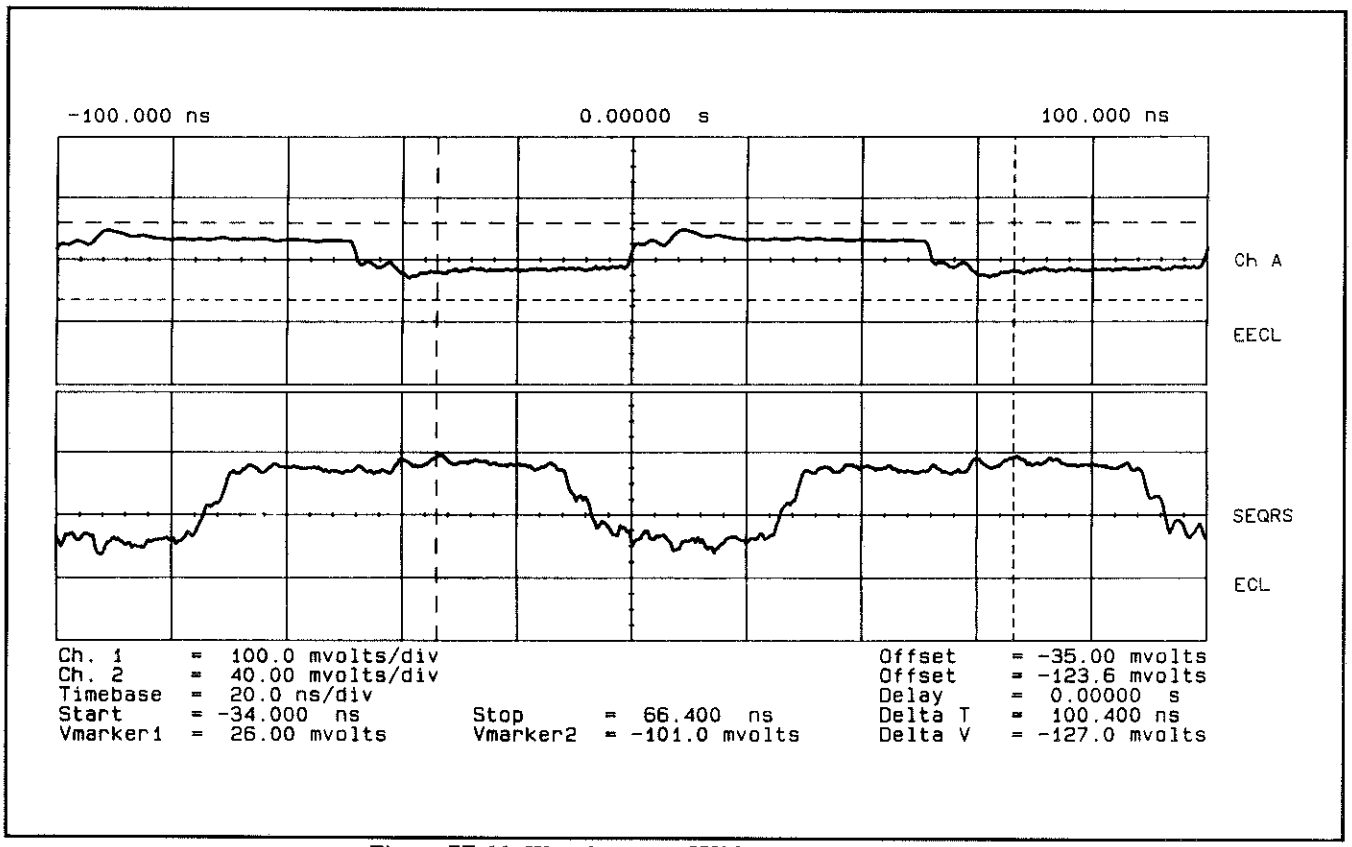


Figure 7E-11. Waveform at A5U29(A4) and A5U29(C11)

B. If both are present, the Sequencer is at fault. Check the A2 board if the Channel A signal is absent. If the SEQ_RS signal appears erroneous, do the following:

1. Verify that MASTER_RS at A5U9(4) is low (ECL level) and that SEQ_GATE_RS at A5U9(5) toggles at 10 MHz (ECL level). See *Figures 7E-12* and *7E-13*. If both signals are correct, change A5U9. Otherwise, if the MASTER_RS is incorrect, change U7 and U9.

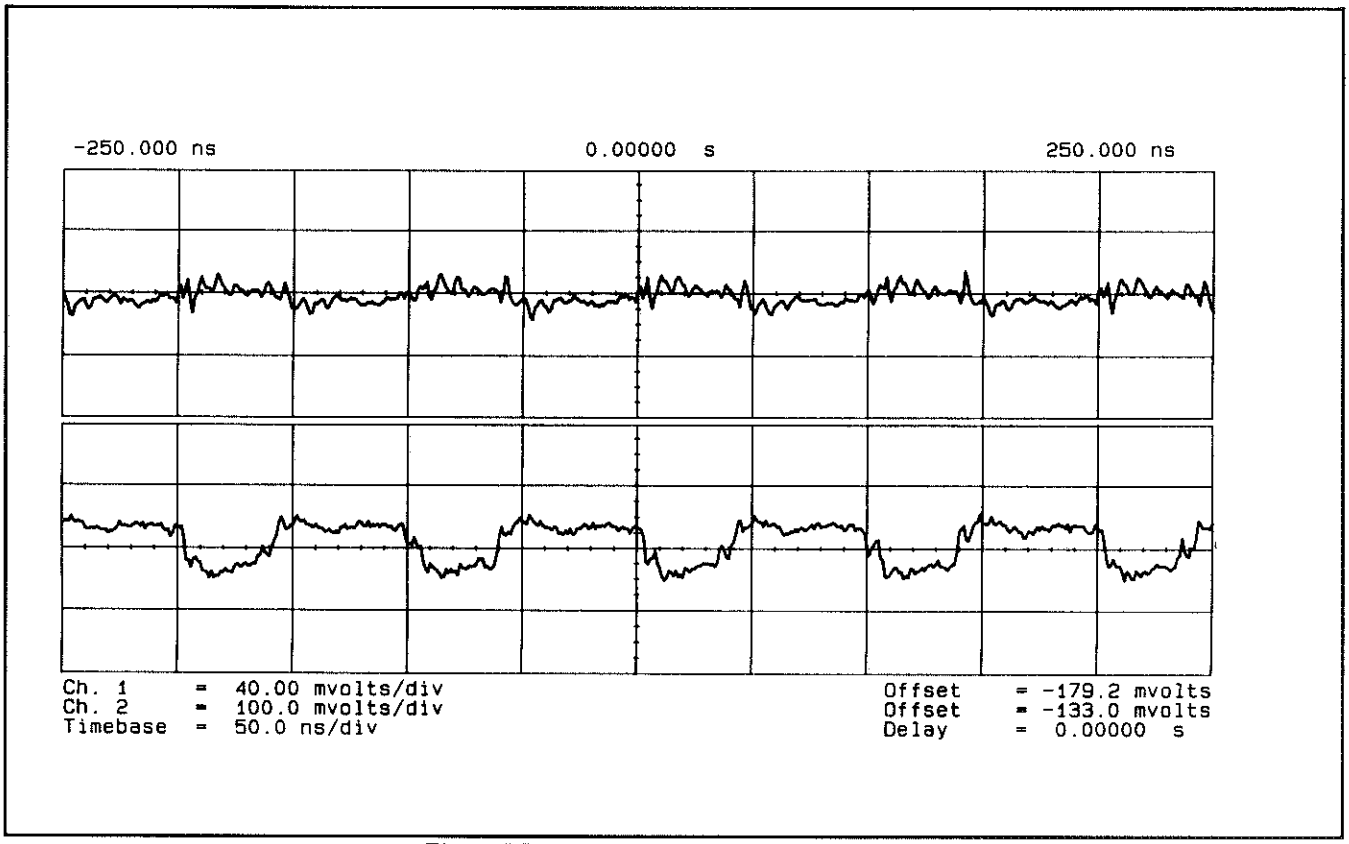


Figure 7E-12. MASTER_RS Signal at A5U9(4)

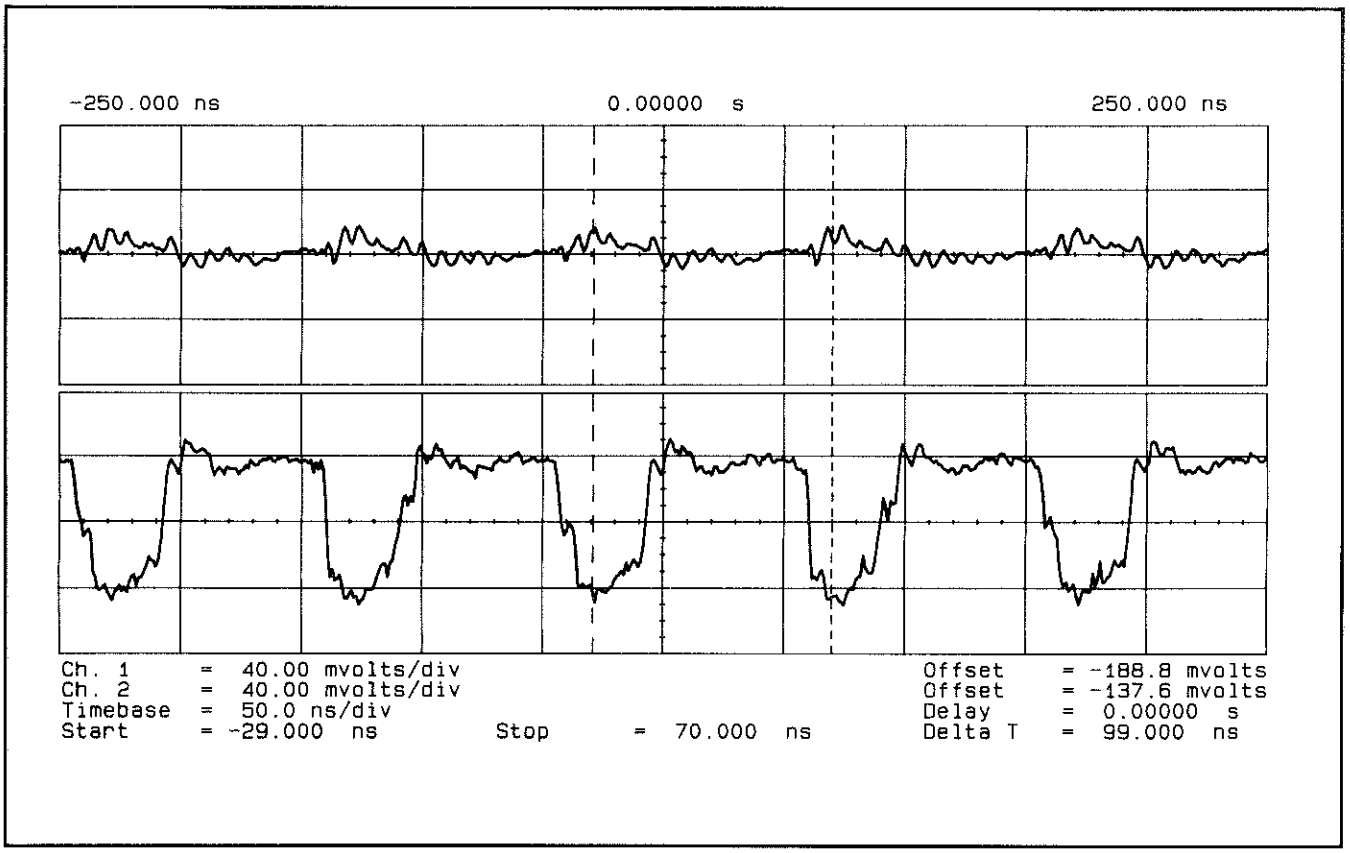


Figure 7E-13. SEQ_GATE_RS at A5U9(5)

2. If the MASTER_RS continues to be incorrect, the trouble lies in the A6 board which generates the ~BMEAS and BFUL_W signals.

3. If, however, SEQ_GATE_RS does not toggle at the correct frequency, then perform the following:

   a. Change U14 and U4. If the problem persists, check the STATE MACHINE, A5U12, as described earlier. If the error still exists, then the trouble lies in the A6 board which generates the SYSIN, the B (S*~T), and the B(S+~T) signals. See *Figures 7E-14* and *7E-15*.

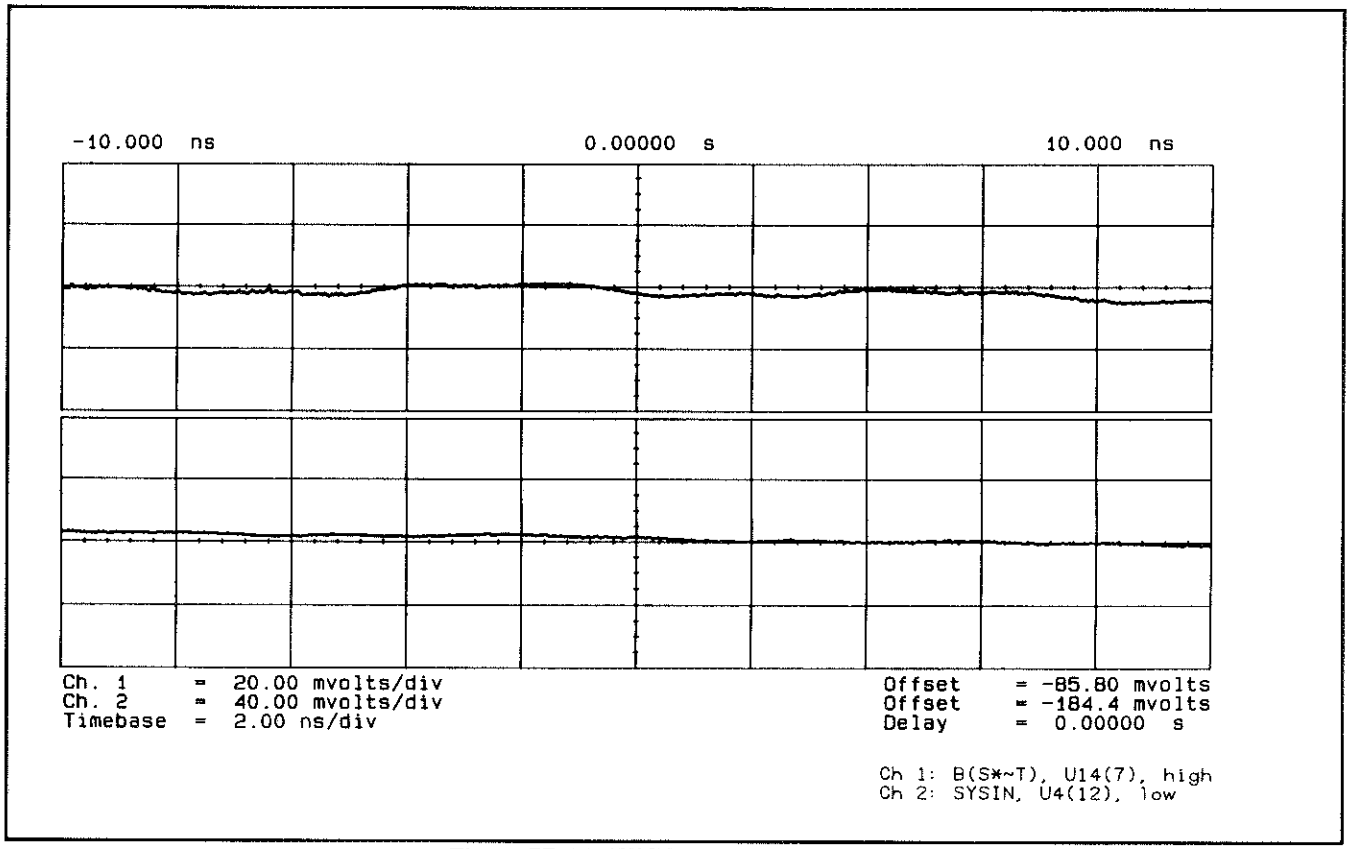


Figure 7E-14. SYSIN and B(S~T) Signals*

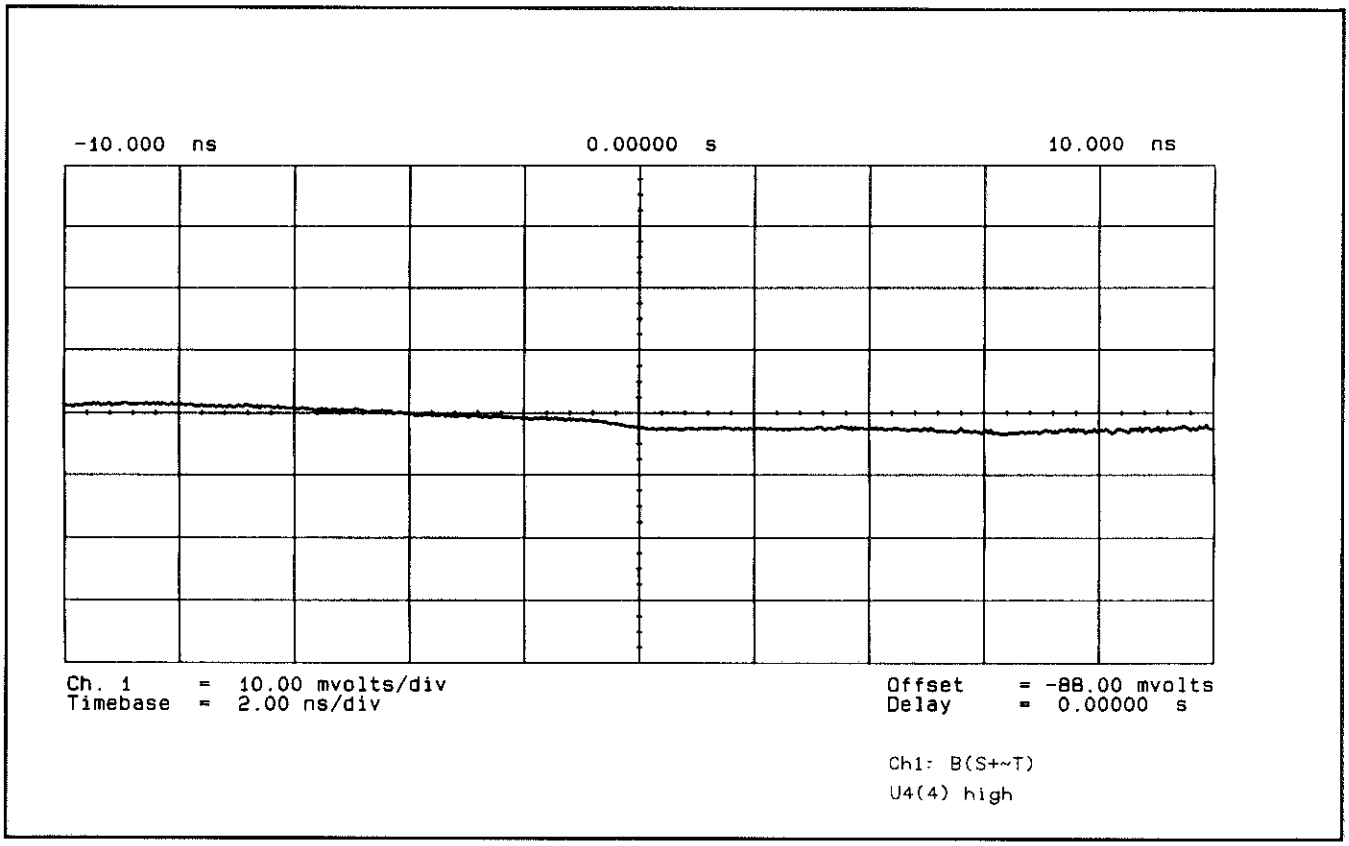


Figure 7E-15. B(S+~T) Signal

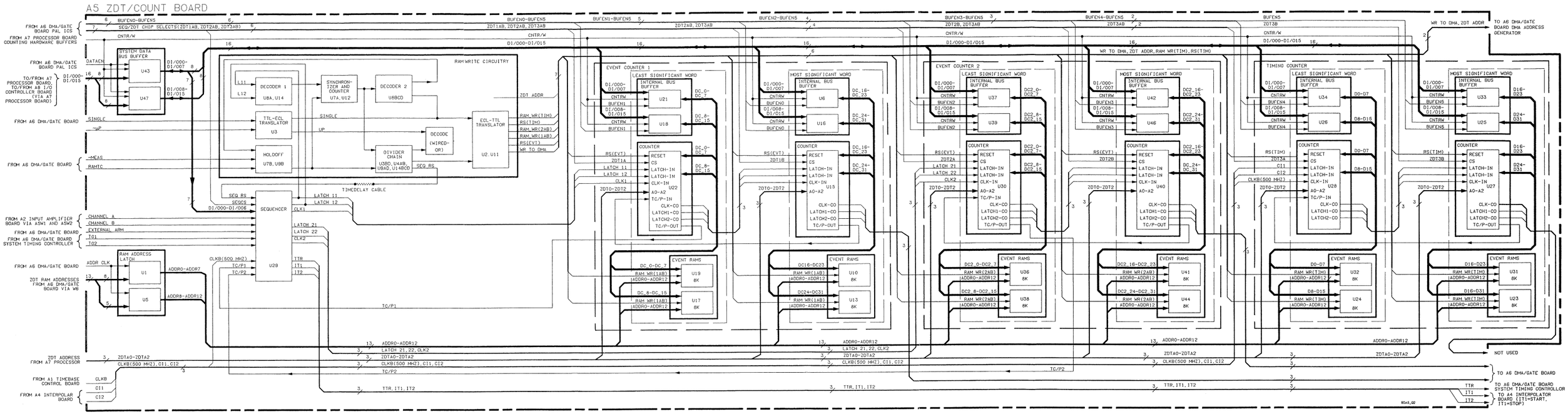
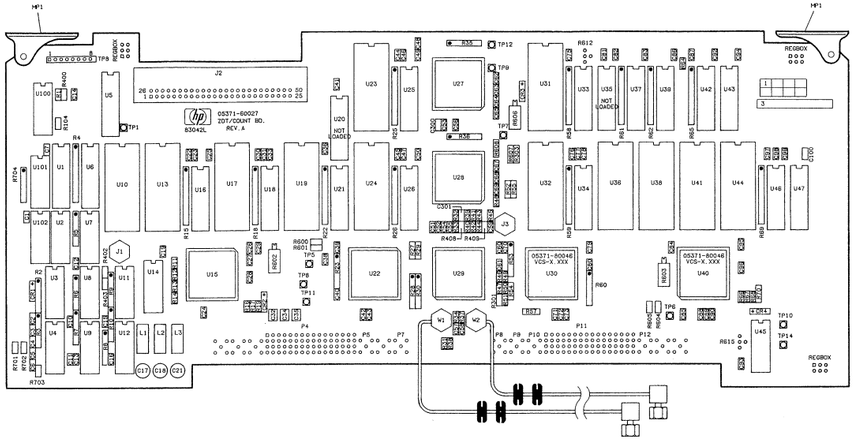


Figure 7E-16. A5 ZDT/Count Board Block Diagram



A5 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A5 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THIS SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

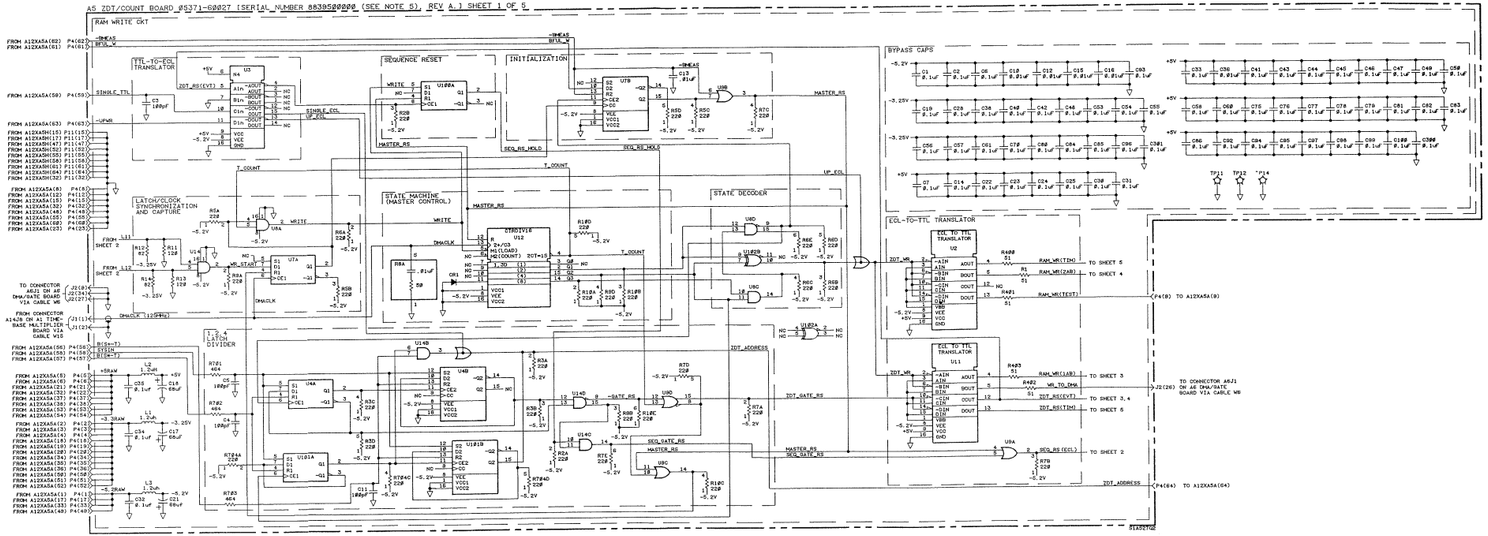
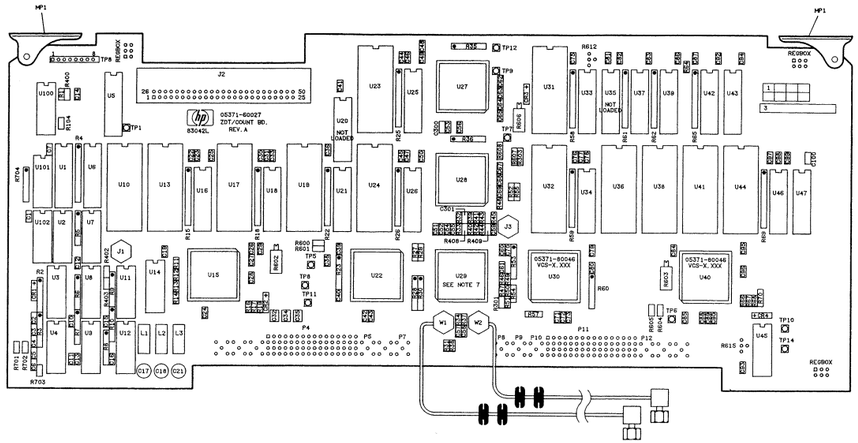


Figure 7E-17. A5 ZDT/Count Board Schematic Diagram (Sheet 1 of 5)



AS SCHEMATIC DIAGRAM NOTES

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2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. COMPONENTS C402,R28,R21 ARE NOT LOADED. VALUES NOT PROVIDED ON SCHEMATIC.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THIS SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.
7. R404, R405, R406 AND R407 ARE LOCATED ON THE BACK OF THE BOARD NEAR U29.

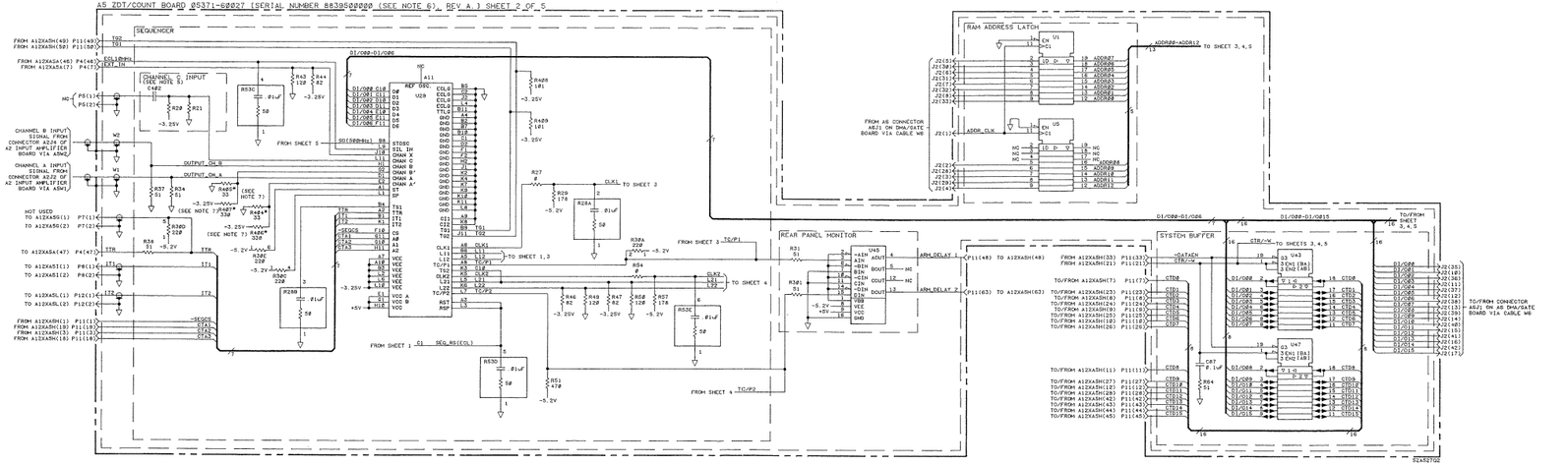
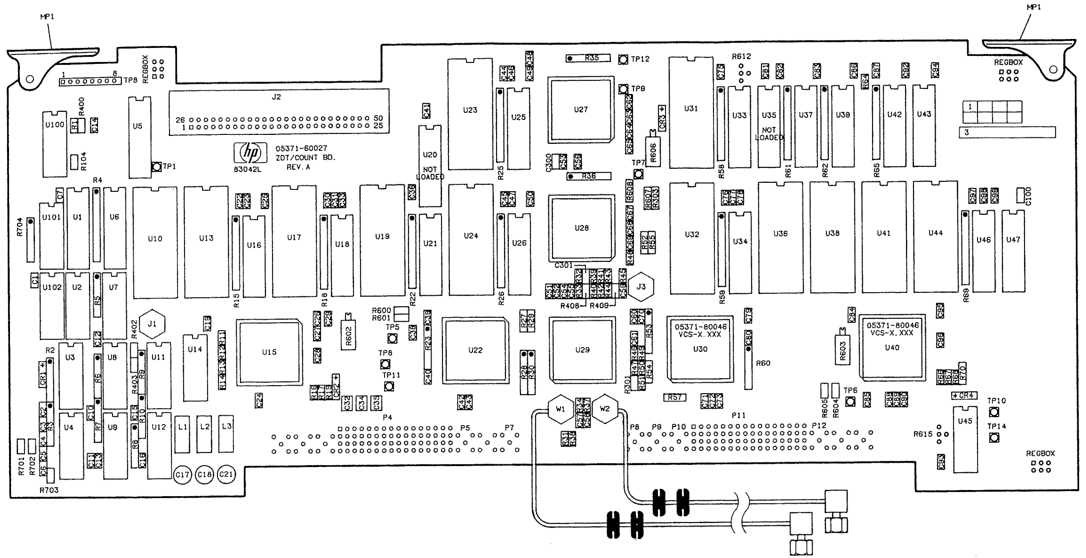
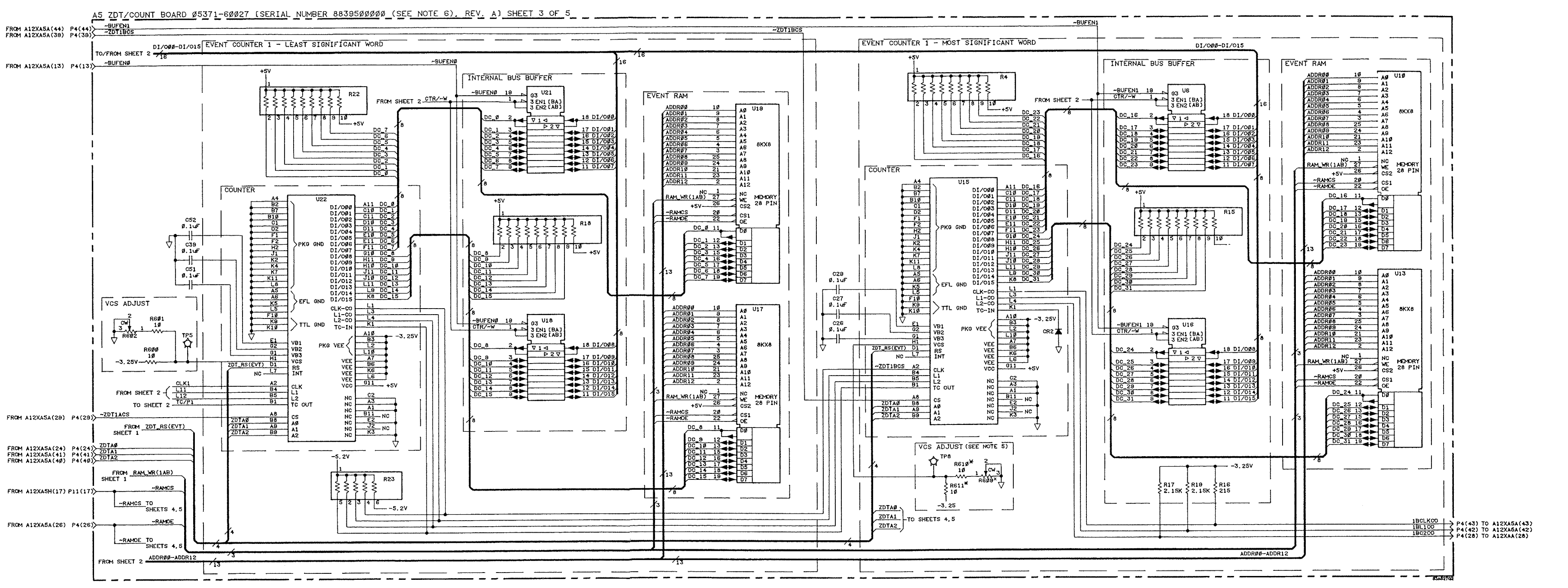


Figure 7E-17. A5 ZDT/Count Board Schematic Diagram (Sheet 2 of 5)





A5 SCHEMATIC DIAGRAM NOTES

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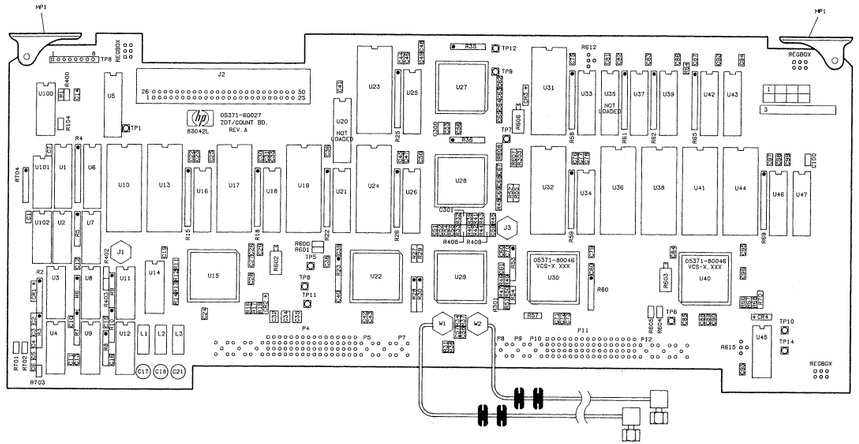
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. RESISTORS R6Ø9-R611 AND TEST POINT TP8 MAY OR MAY NOT BE LOADED.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

Figure 7E-17. A5 ZDT/Count Board Schematic Diagram (Sheet 3 of 5)



A5 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A5 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. RESISTORS R615-R617 AND TEST POINT TP10 MAY OR MAY NOT BE LOADED.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THIS SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICTION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

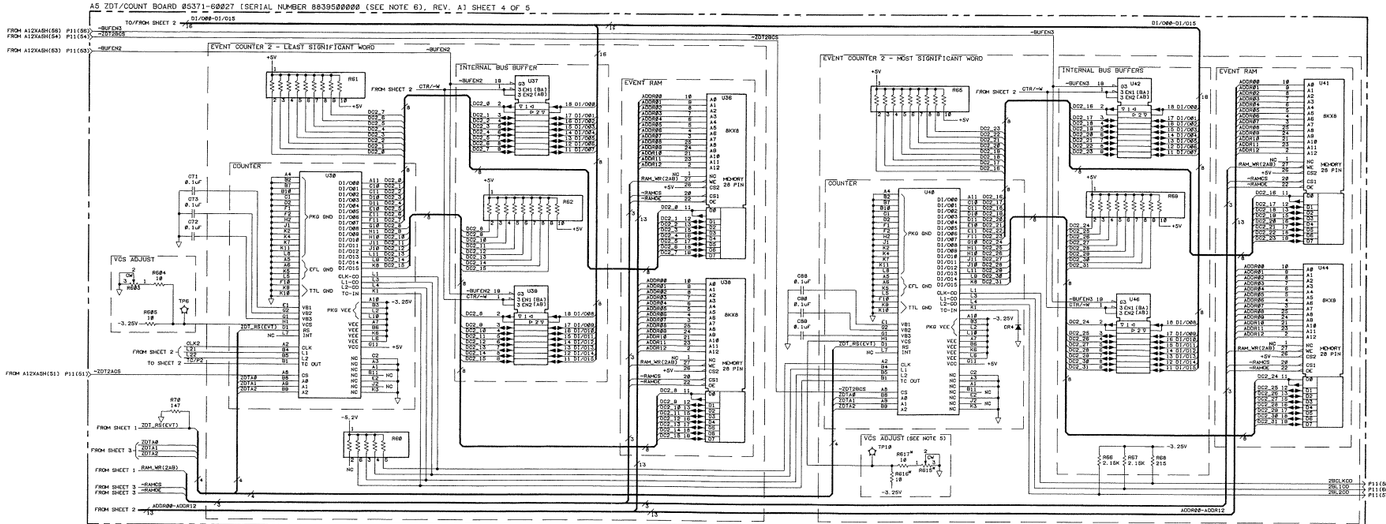
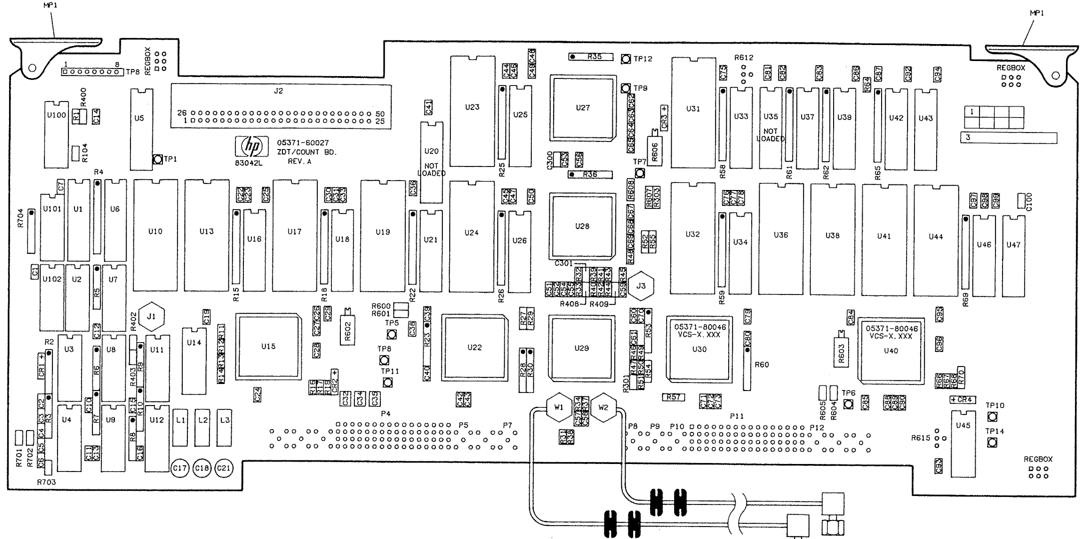
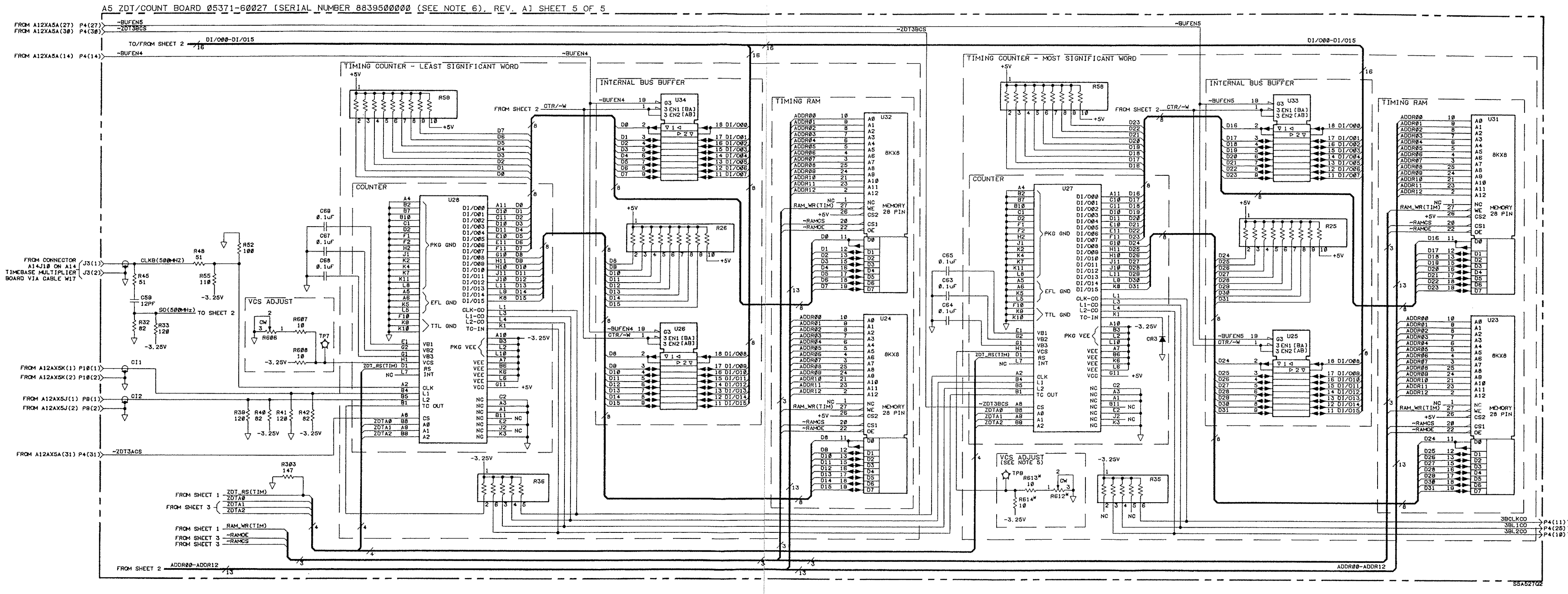


Figure 7E-17. A5 ZDT/Count Board Schematic Diagram (Sheet 4 of 5)





A5 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A5 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. RESISTORS R612-614 AND TEST POINT TP9 MAY OR MAY NOT BE LOADED.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THIS SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED_CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

Figure 7E-17. A5 ZDT/Count Board Schematic Diagram (Sheet 5 of 5)

SECTION 7F
A6 DMA/GATE BOARD

7F-1. A6 DMA/GATE BOARD

7F-2. Introduction

Together, the A5 ZDT/Count and A6 DMA/Gate Boards execute and control the HP 5371A counting process. The A6 DMA/Gate Board's main functions are the generation of DMA addresses, and the control of reading and writing measurement and interpolation data to and from more than fourteen RAM ICs located on the A5 ZDT/Count and A6 DMA/Gate Boards. Other important functions of the board include the following:

- Generation of the Gate Timer signals, TG1 and TG2, by the *System Timer Controller* (STC) for use by the A5 ZDT/Count Board's *Sequencer* IC to gate latch signals during INTERVAL Arming mode,

- Temporary storage of interpolation data generated by the A4 Interpolator Board in the *Start and Stop Interpolator RAMs*,

- Controls generation of RAM memory addressing by the *Dump Mode Counter* when unprocessed binary data is read and sent directly to an external controller via the HP-IB interface bus, and

- Buffers, shapes, sets trigger level voltage, and translates front-panel EXTERNAL ARM input signal by the *EXTERNAL ARM Input Amp* prior to routing signal to the A5 ZDT/Count Board's *Sequencer* IC for use during EXTERNALLY GATED Sampling.

The A6 DMA/Gate Board has twelve circuit blocks: (1) *DMA Address Generation*, (2) *DMA Input Buffers*, (3) *Control Word Latches*, (4) *Dump Mode Counter*, (5) *System Timing Controller (STC)*, (6) *Interrupt Generation PAL*, (7) *ZDT Address Generation*, (8) *Start and Stop Interpolator RAMs*, (9) *PAL Decode Section*, (10) *Totalize Circuitry*, (11) *Overflow Detection Circuit*, and (12) *EXTERNAL ARM Input Amp* circuit. The component-level theory for the blocks listed follow. See "A6 DMA/Gate Board Block Diagram" in *Figure 7F-1* for reference.

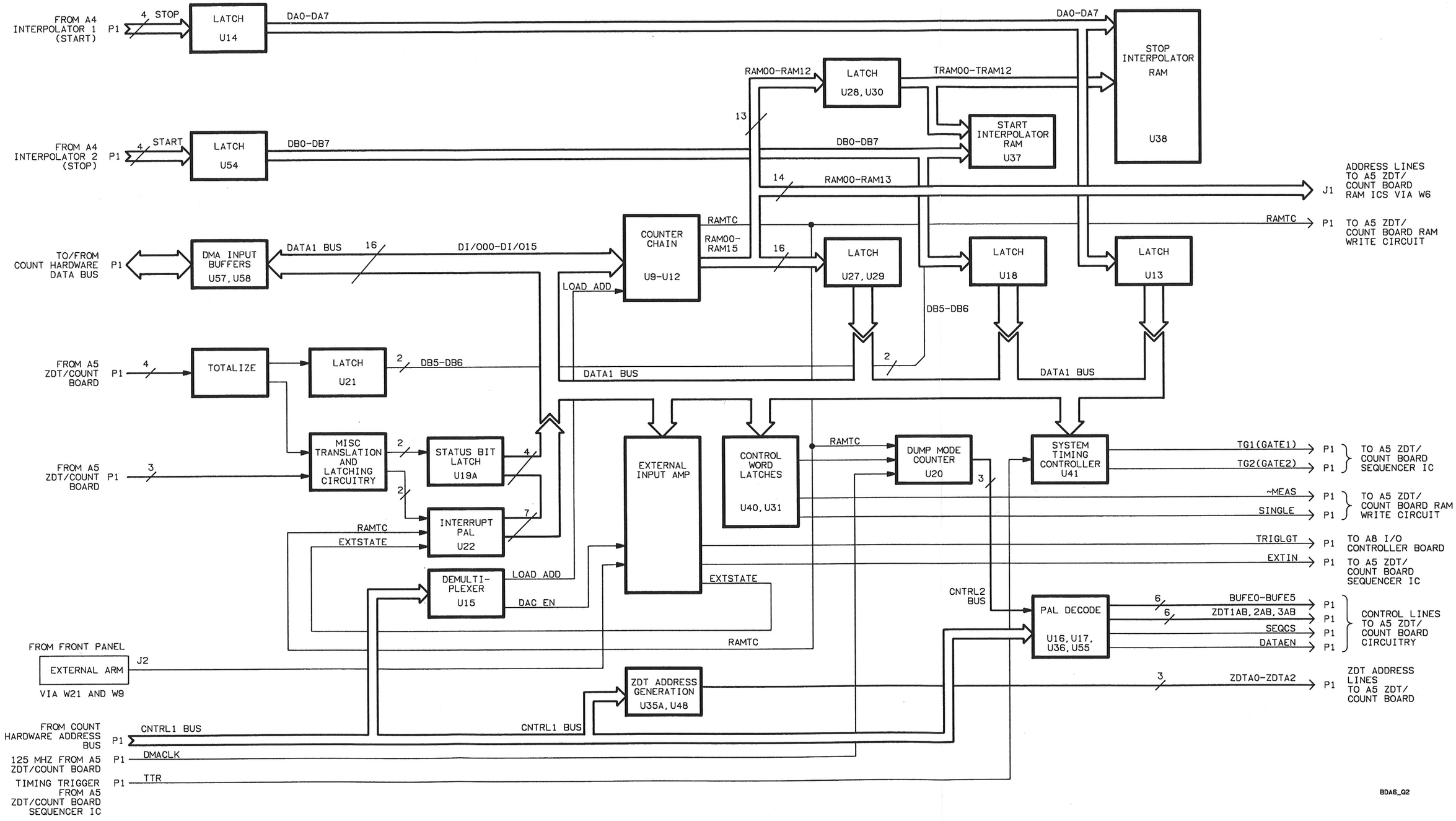


Figure 7F-1. A6 DMA/Gate Board Block Diagram

7F-3. DMA Address Generation

The DMA Address Generation circuitry is comprised of the Counter ICs A6U9 through A6U12, address latches A6U28-U30 and a duplicate pair on the A5 ZDT/Count Board (A5U1 and A5U5).

Latches A6U28 and U30 latch the counter outputs and provide address lines, TRAM00-TRAM12, to the *Start* and *Stop Interpolator RAMs*, A6U37 and U38 respectively. Latches A5U1 and A5U5 in a similar way provide addresses to the measurement RAMs located on the A5 ZDT/Count Board. At the beginning of each measurement block, the 68000 μP places a 16-bit word (DI/O00-DI/O15) at the inputs of the address counters. The thirteen low-order bits represent the measurement and interpolator RAM address at which the first measurement result will be stored (The three high-order bits are set to logic high). The 68000 μP then generates an active-low counter load pulse, LOAD ADD, and applies it to the address counters via decoder A6U15 (pin 14). This latches the initial memory address into the address counters. The load signal is sufficiently delayed by AND gate A6U2A to allow the data just loaded to settle at the counter outputs before being clocked onto bus lines RAM00-RAM12. The leading edge of the delayed counter load signal (LOAD ADD), now called ADD CLK, clocks both address latch pairs; A6U28 and A6U30, located on the DMA/Gate Board, and A5U1 and A5U5, located on the A5 ZDT/Count Board. This places the data previously loaded in the address counters and now on bus lines RAM00-RAM12 on the A6 assembly's Interpolator RAM Address Bus (TRAM00-TRAM12) and the A5 assembly's measurement RAM address bus (ADDR00-ADDR12). Inverters A6U6A and B apply additional delay to the load pulse before it clocks the address counters. This places the address counter output on the RAMA00-RAMA12 bus. This process causes the address counters to be numerically one greater than the latched outputs.

Once the *DMA Address Generation* circuitry has initialized, the address counters are incremented and the address latches are clocked by measurement write pulse, WR_TO_DMA. This pulse is generated by the *RAM Write* circuit located on the A5 ZDT/Count Board. WR_TO_DMA is ANDed with load pulse LOAD ADD and the terminal count signal of the *Dump Mode Counter*, INCRDADD. While the WR_TO_DMA write pulse is low, measurement data is written to the measurement RAM and interpolator RAM location addressed by the address latches. The rising edge of WR_TO_DMA causes the next address to latch into the address latches and increments the address counter by one. The WR_TO_DMA signal continues to increment the address counters until the terminal count is reached. The output at pin 12 of A6U12, the highest order address counter, generates signal FUL_W which identifies a terminal count condition. A6U1A output, RAMTC, which is the FUL_W signal delayed by one write cycle, ensures that the *INTERRUPT PAL* circuit (A6U22) generates a 68000 μP interrupt (~INT1) AFTER the last set of measurement data is loaded into memory.

Address latches A6U27 and U28 are also part of the *DMA Address Generation* circuit. These latches place the address counter's outputs on the DMA/Gate board's DATA_1 data bus. Here the data can be read by the 68000 μP. A control signal from *PAL Decode* IC A6U16 (pin 18) enables both latches, placing RAMA00-RAMA15 bits on the DATA_1 data bus, lines DI/O00-DI/O15. This data's usefulness is limited to 5371 diagnostics and troubleshooting.

7F-4. DMA Input Buffers

The bidirectional *DMA Input Buffers* A6U57 and U58 connect the DMA/Gate board's DATA_1 data bus to the Count Hardware Data Bus (CTD0-CTD15). The direction of data flow through the buffers is controlled by the 68000 μP's count read/write signal CTRW. When CTRW is logic high, the buffers allow the DMA/Gate board to pass data from its own DATA_1 Bus to the Count Hardware Data Bus. When CTRW is logic low, the buffers allow data to pass from the Count Hardware Data Bus to the DMA/Gate Board's DATA_1 Bus. *PAL Decode* IC A6U16(pin 13) DATBU signal controls both buffer enable lines. DATBU is at logic low during all data transfers. Setting DATBU to a logic high, isolates the Count Hardware Data Bus from the DMA/Gate board's DATA_1 data bus.

7F-5. Control Word Latches

Control word latches A6U40 and U31 latch the control word generated by the A7 board's 68000 μP from the DMA/Gate board's DATA_1 data bus. Their outputs are used as control signals on both the A6 DMA/Gate and A5 ZDT/Count Boards. The 68000 μP clocks the control word latches via decoder A6U15 (pin 7). Some examples of the

duties performed by the control signals include the following:

- Setting Up the *Dump Mode Counter's* initial value,
- Enabling of the *Dump Mode Counter*,
- Informing circuitry as to when a measurement is being taken,
- Controlling of the ECL-level 10MHz signal to the A5 ZDT/Count Board, and
- Resetting several ICs located on both the A5 and A6 assemblies.

7F-6. Dump Mode Counter

A dump operation is the transfer of unprocessed binary measurement data from the A5 ZDT/Count Board's measurement RAMs and A6 DMA/Gate Board's *Start and Stop Interpolator RAMs* to an external controller via the A8 I/O Controller Board's *HP-IB Control Circuit*. A6U20, the *Dump Mode Counter*, sequentially selects the measurement RAMs and buffers used during dump mode. Prior to the start of each memory dump, the appropriate starting memory address is latched by the *DMA Address Generation* address latches, and the 68000 μP sends a control word to the *Control Word Latches*, A6U40 and U41. The control word latch provides the *Dump Mode Counter* with an initial starting value (DUMPA0-DUMPA2). The initial value set up at the counter's inputs depends on the TYPE of measurement data being dumped. The control word also ensures 68000 μP control of the *Dump Mode Counter*'s enable line by setting control signal DUMPMO [A6U40 (pin 16] to logic high. DUMPMO is then ANDed with control signal ~Meas. ~MEAS is low ONLY when a measurement is in progress. ANDing the two means that the *Dump Mode Counter* is active only when the HP 5371A is no longer performing a measurement. The output of AND gate U3C (pin 8) is inverted and and applied to OR gate A6U23B where it is ORed with terminal count RAMTC. ORing the two signals disables the *Dump Mode Counter* after the last measurement sample has been passed to the external controller. The OR gates output, DUMPV, is ORed with 68000 μP control signal ~CHDMA at OR gate A6U23C. If DUMPV is a logic high, the *Dump Mode Counter* is disabled. If DUMPV is a logic low, then the 68000 μP determines the state of the counter's enable line, DUMPEN.

Having set an initial value at A6U20 inputs (pins 1,10, and 15) and turned control of the DUMPEN signal over to the 68000 μP, the 68000 μP generates a load pulse at decoder A6U15 (pin 15). This load pulse is ANDed with two other signals, ~RESET and a delayed version of A6U20 (pin 12) terminal count, which can also load the *Dump Mode Counter*. The counter outputs, DUMPA4-DUMPA6, are decoded and buffered by *PAL Decode* ICs A6U36 and U55. The PAL outputs, in turn, sequentially enable the appropriate buffers, measurement and interpolator RAMs indicated by the counter's output. Once the measurement data has been read (dumped) from the specified RAM address, the *Dump Mode Counter* is incremented by the DMACLK line. This process repeats itself until the *Dump Mode Counter* terminal count is reached [A6U20 (pin 12)]. When the terminal count is reached, the output at pin 12 of A6U20 (INCRDADD) clocks the *DMA Address Generation* counters to the next address. The A6U20 (pin 12) output is also delayed by A6U56C and used to reload the *Dump Mode Counter* with its initial value. Therefore, the same RAMs are again selected for dumping but at a new address. This cycle continues until all specified RAMs have been read (or dumped).

7F-7. DUMP MODE EXAMPLE

Consider a Time Interval A is B measurement. This measurement requires the use of A5 ZDT/Count Board *Timing Counter* ZDT chain and A4 Interpolator. *Dump Mode Counter* A6U20 is loaded with an initial value of four. The binary four is decoded by the *PAL Decode* IC A6U55 which enables the A5 assembly's *Timing Counter* ZDT chain. The decoded output of *PAL Decode* IC A6U36 enables the appropriate buffers that place the low-order time measurement RAMs onto the data bus. From here the data is sent to the A8 I/O Controller Board's *HP-IB Control Circuit* for processing by an external controller. Once the data has been sent out over the HP-IB bus, *Dump Mode Counter* A6U20 is incremented to binary five by the DMACLK line. The five indicates to the PALs that the high-order time ZDTs should be placed on the data bus. Next, the counter is incremented to six, which places the A6 Interpolator RAM data on the data bus. The counter is now clocked to binary seven where a terminal count is generated at U20 pin 12. The terminal count increments the measurement memory address via INCRDADD, and sets the *Dump Mode*

Counter back to its initial value of binary four. This process repeats itself for the next memory address location and continues until all measurement data has been dumped.

7F-8. System Timing Controller (STC)

The System Timing Controller (A6U41), or STC, provides two identical, individually programmable gate timing signals, TG1 and TG2. TG1 or TG2 provide start and stop arming signals to the Sequencer IC, A5U29, located on the A5 ZDT/Count Board. Each signal is a continuous series of pulses having equal rising edge-to-rising edge periods that correspond to the "gate time" of the measurement. The "gate time" represents the time during which measurement data is taken. The period of each signal is is controlled by the 68000 μP via the A6 DATA_1 bus, lines DI/O00-DI/O15, from inputs supplied from either the instrument's front panel or over the HP-IB interface. The period of TG1 or TG2 is programmable from 600 ns to 8.0 s.

TG1 and TG2 gate signals are used when the HP 5371A is set up to make continuous gating measurements while in Interval Sampling, Edge/Interval, or Time/Interval arming modes only.

The STC derives its reference clock from the 10 MHz source provided by the A1 Timebase Control Board. A6U59B divides the 10 MHz signal by two and routes it to pin 6 of the A6U41. ICs A6U59A and U3D work together to ensure that the 5 MHz signal clocks the STC IC only when its chip select signal, GATECS, is pulled low. Internal STC circuitry can be programmed to divide (or "prescale") the 5 MHz clock input by either 1000, 100, 10, or 1, allowing pulse width resolution of 200 ns, 200 us, 20 us, or 2 us. This frequency serves as a timebase for the internal counters that ultimately generate the TG1 and TG2 pulses. The FOUT output, pin 7, is derived from a four-bit counter that can be programmed to divide any integer value from 1 through 16. The input to the divider is the frequency scaler output. FOUT is routed to the SOURCE input, pin 5, for counting by the internal counters.

The circuitry that generates the gate pulse necessary to start the STC counting process is comprised of latches A6U32A, U32B, U42A, U42B, U47, and U50. The A5 Sequencer sends a TTR (Timing Trigger) edge when all arming conditions have been met telling the STC to start the counting process. A6U42A synchronizes the TTR edge to the STC Gate input and ensures minimum Gate pulses to A6U41 (pins 4, 39, 36,35, and 34) of 200 ns. To synchronize the internal counter's input clock with the TTR signal from the A5 ZDT/Count Board, FOUT also clocks flip-flops A6U42A, U42B, and U32B. The ECL-level TTR signal is translated to TTL level by A6U50 and placed at the data input of A6U42A. TTR remains setup at A6U42A until synchronization occurs. After synchronization occurs, A6U42 (pin 5) goes high and is applied to the STC GATE inputs. This starts the counting process with the STC. Once counting has begun, TTR is delayed three clock cycles (600 ns) by latches A6U42B, U32A, and U32B. This delay compensates for hardware delays introduced by the STC IC itself. TTR is delayed by approximately 800 ns by the time it reaches the common strobe pin 6 of TTL-to-ECL translator A6U47. The first INTERVAL therefore begins <800 ns after the HP 5371A measurement is armed. The STC's initial gate timer pulse is artificially injected at the start of the measurement, by a delayed version of the TTR signal, causing the first TG1 or TG2 period to include STC initialization delays. Enabling A6U47 passes TG1 and TG2. The STC's OUT outputs go low only after the appropriate counter chain has reached its pre-programmed terminal count. Each time the STC's OUT output pins are set low while the TTR line is high, a gate time pulse (TG1 or TG2) is generated at pins 14 or 15 of A6U47.

7F-9. Interrupt Generation PAL

Interrupt Generation PAL A6U22's primary function is to monitor when a block of measurements has completed and notify the 68000 μP of its completion by generating an interrupt signal, ~INT1. Status bits also monitor the status of EXTERNAL ARM Input Amp, measurement RAM terminal count, and Channel A & B event counter chain overflow status bits. The status bits are placed on the DATA_1 data bus when ~INTRD signal is set to logic low.

7F-10. ZDT Address Generation

A6U48 is a quad 2:1 multiplexer that provides address lines ZDTA0-ZDTA2 for the ZDT's located on the A5 ZDT/Count Board. The multiplexer is gated by the ~MEAS line. When ~MEAS is a logic "high", lines CTA1-CTA3 appear on the ZDT address lines, ZDTA0-ZDTA2. A high on ~MEAS indicates that the HP 5371A is not performing a measurement. While measurements are not being made, the 68000 μP has control of the ZDT address lines via lines

CTA1-CTA3. But during a measurement, it is desirable to read ZDT latch 1 and 2 without microprocessor intervention to change the ZDT address. This is accomplished by pulling multiplexer input pins 5 and 11 high and controlling input pin 3 via signal ZDT_Address generated on the A5 ZDT/Count Board. ZDT_Address is held at ECL level "high" during single channel measurements and toggles high and low for dual channel measurements. A6U35A XORs the TTL equivalent of ZDT_Address, ZDTADDIN, with signal ~LI_EN. ~LI_EN is set high for single-channel measurements and low for dual-channel measurements. XOR gate output, A6U35A (pin 3) enters the pin 2 of multiplexer A6U48 and becomes the lowest-order ZDT address bit, ZDTA0. Therefore, ZDT address lines are always a binary 110. For dual-channel measurements, the ZDT address cycles between binary 111 and 110.

7F-11. Start and Stop Interpolator RAMs

A6U37 (Start) and A6U38 (Stop) Interpolator RAMs store the 4-bit A4 Interpolator Board data and two totalize status bits latched from the A6 *Totalize* circuit. Buffers A6U54 and A6U14 respectively to the start RAM data bus DB0-DB7 and the stop RAM data bus DA0-DA7. When the interpolator data is valid, control signal INT_BSEN enables both buffers, placing the interpolator and totalize data at the Interpolator RAM inputs. The 68000 μP then control signal INTRCS which enables the appropriate RAM. The WR_TO_DMA signal, generated by the A5 assembly *RAM Write Circuit*, writes the data into the RAM location address setup by address latches A6U28 and U30. When data is read from the interpolator RAMs, buffers A6U14 and U54 are disabled and the bidirectional buffers A6U13 and U18 are enabled. This routes data from the RAMs directly to the Data_1 data bus. The 68000 μP controls the direction of data flow via signal CTRW.

7F-12. PAL Section

Four uniquely programmed PAL ICs decode address and control signals originating on the A7 Processor Board and provide control signals to the A5 ZDT/Count and A6 DMA/Gate Boards. A6U17 allows independent enabling of the A5 assembly's Sequencer and ZDT counter ICs. A6U36 allows independent enabling of the A5 ZDT/RAM address buffers. A6U55 selects either the A6 Interpolator RAMs. Finally, A6U16 produces miscellaneous control signals which are used throughout the DMA board.

7F-13. Totalize Circuitry

The Totalize function counts the number of events on the input signal during a specified period of time, between a pair of designated edges, or between key pressings of the MANUAL ARM key. Totalize measurements are sampled differently from Frequency/Period measurements. For Totalize measurements, the sampling is synchronous with the interval, edge, or manual key-press, depending on the arming mode. The sampling point is not synchronous to the trigger event. At the A5 ZDT/Count Board count hardware level, this means that sample latches and events (CLK1 and CLK2) are asynchronous. The *Totalize* circuit overcomes this by monitoring Event Counter 1B and 2B latch-carryout signals (1BL1CO, 1BL2CO, 2BL1CO, and 2BL2CO). A latch-carryout is generated when each respective ZDT counter receives a latch signal before a clock (event) signal. Therefore, a logic "high" on the latch-carryout line at the end of a write means that an event clock (CLK1 or CLK2) came during a write. This means that the data stored would be erroneous by ±1 count. The *Totalize* circuit latch, A6U39A, latches the ZDT counter latch-carryout signal at the end of each write and stores it with the 4-bits of interpolator data in the *Start Interpolator RAM*. Because of the propagation delays introduced by the A5 ZDT/Count Board's counting chains, an event clock that occurs right at the end of a write will not cause a latch-carryout to go "high" immediately. Therefore, the *Totalize* latches after the write by an amount equal to maximum ZDT count chain delay. The write pulse, WR_TO_DMA, is delayed by approximately 50 ns by A6U7, before clocking latch A6U39A. If the latch-carryout signal is at logic "high" prior to being latched by the delayed write pulse, the write data is interpreted as being correct. But if the latch-carryout signal is at "logic" low when latched, the data could be erroneous. The possibility of introducing ±1 count error during Totalize measurements is overcome by writing the measurement data into RAM more than once. Writing twice gives at least one valid set of data since the event clock that arrives during the first write is latched and ensures correct data during the second write.

A6U39A outputs are routed through buffer A6U21 to the Start and Stop Interpolator RAMs.

7F-14. Overflow Detection Circuit

The detection of ZDT counter IC overflow condition is performed by the *Overflow Detection* circuit and a software routine contained in the HP 5371A firmware. Signals 1BCLKCO and 2BCLKCO represent the most significant bit (i.e 32nd bit) from Event ZDT counters 1B and 2B. ECL-to-TTL translator A6U52 latches these two signals when ZDT_ADDRESS goes active, which is generated by the A5 *RAM Write* circuit, to the data input pins of latches A6U34AB and U33AB. Latches A6U33A and A6U33B are clocked by the TTL version of signals 1BCLKCO and 2BCLKCO respectively. Both latched outputs go the *Interrupt Generation PAL*, A6U22, where they are decoded and generate a 68000 μP interrupt (~INT1). Latches A6U34A and U34B inform the microprocessor as to when the overflow occurred, before or after the latch signal. Latch A6U34AB outputs are read by the 68000 μP via *Status Bit Latch* A6U19A. Any overflow detected is compensated for by the HP 5371A firmware.

7F-15. EXTERNAL ARM Input Amp

The *EXTERNAL ARM Input Amp* block is a 100 MHz amplifier that buffers, shapes, and translates to ECL logic levels the front-panel EXTERNAL ARM input signal, and then route it to the A5 ZDT/Count Board's Sequencer IC, A5U29, for use during externally gated sampling.

The *EXTERNAL ARM Input Amp* has five stages: (1) a signal conditioning stage, (2) a high and low frequency amplifier stage, (3) a Schmitt stage, (4) a buffer stage, and (5) a digital-to-analog stage (DAC).

7F-16. SIGNAL CONDITIONING STAGE

The input impedance of the *EXTERNAL ARM Input Amp* is 1 MΩ (nominal), shunted by less than 50 pf. The 1 MΩ impedance is set by resistors A6R3, R4, R10, and R9. These resistor also perform other functions. A6R3 provides high frequency line matching and transient input protection. A6R4 and clamping diodes A6CR3 and CR4 provide over-voltage protection to the *EXTERNAL ARM Input Amp* stage. To reduce distortion caused by high amplitude input signals, resistors A6R4, R10, and R9 form a voltage divider such that the signal level drops 24% across A6R4. This prevents A6Q2 and Q10 from going into saturation with a 5 V p-p input signal. Capacitor A6C5 compensates the divider.

7F-17. HIGH AND LOW FREQUENCY AMPLIFIER STAGE

The high and low frequency amplifier stage consists of parallel high and low frequency buffering circuits. The high frequency path consists of an impedance converter circuit with an AC gain of approximately 0.9 and a bandwidth of approximately 100 Hz to greater than 100 MHz. The low frequency path provides DC trigger level control. The low frequency path also has an AC gain of 0.9 but has a bandwidth from DC to approximately 100 kHz.

In the high frequency path, the external arming signal is AC coupled, via A6C8, to the FET A6Q1 gate. A6Q1 converts the high impedance at the circuit input to a low impedance at the FET source. Resistor A6R15 biases the FET to saturation and resistor A6R16 buffers A6Q3 to prevent it from oscillating. Additional current is provided via pull-up resistor A6R17 to increase the speed of positive voltage swings at the FET source with instantaneous trigger level voltage changes. Resistor A6R23 sinks current from emitter-follower A6Q3. The signal from the output of A6Q3 is fed through the low frequency circuit and input back to the base of A6Q3.

In the low frequency path, operational amplifier A6U26, transistors A6Q2 and Q3 operate together as a differential feedback amplifier. The signal is DC coupled to the op-amp input at pin 2. A voltage from either from a digital-to-analog circuit (DAC) is routed to the op-amp input at pin 3. Capacitor A6C24 provides external frequency compensation. On the trigger level control voltage line, A6R21 and C26 form a low-pass filter to keep out digital noise generated by DAC IC A6U46. At the output of A6U26, resistor A6R12 limits the base drive to transistor A6Q2 and combines with A6R13 and C21 to filter out noise on the –5.2 Volt supply line. A6R13 performs the additional function of stabilizing A6Q2 at high temperatures.

Common-emitter transistor A6Q2 operates simultaneously as a low frequency amplifier and as a current source for FET A6Q8 in the high frequency circuit. The current to the FET is determined by the emitter resistor A6R14. The

inverted signal at the collector of the common-emitter A6Q2 is summed with the high frequency signal at the source of A6Q1 and sent through emitter-follower A6Q3.

The signal gain of the low frequency circuit is determined by feedback resistor A6R11 and op-amp resistors A6R20, R10, and R9. The values of these resistors are chosen to provide a gain equal to the high frequency gain of approximately 0.9.

Resistors A6R11, R20, R10, and R9 also determine the 1.8 DC gain for the trigger level control voltage. This control voltage from DAC IC A6U46 is programmable from -2.5 to +2.5 Volts. The corresponding level shift at the emitter of A6Q3 ranges from -4 to +4 Volts and cancels out any DC component of the EXTERNAL ARM input signal.

7F-18. SCHMITT STAGE

The *Schmitt* stage receives the analog signal from the high and low frequency amplifier and converts it to an ECL level square wave output. The output signal, EXT IN, is sent to the A5 ZDT/Count Board's Sequencer IC, A5U29, for use during externally gated sampling. It also provides fixed control of the counter's EXTERNAL ARM input channel sensitivity.

The major component in this circuit is the high speed comparator A6U43. The comparator offset is set by resistors A6R32 and R33. The offset is factory-set at approximately +20 millivolts from the zero volt trigger point.

It should be noted that the *Schmitt* stage always triggers at zero Volts. Setting the trigger level of the EXTERNAL ARM input does not change the trigger point on the Schmitt. The trigger level control along with the high-low frequency amplifier stage compensates for the DC level of the EXTERNAL ARM signal and shifts it to zero Volts.

The comparator's complementary ECL outputs are buffered by resistors A6R35 through R37. Resistors A6R104 and R103 provide a current sink for the output lines to the -5.2 Volt supply.

7F-19. EXTERNAL ARM TRIGGER SLOPE STAGE

The *EXTERNAL ARM Trigger Slope* stage s comprised of an Exclusive-Or gate which XORs the *Schmitt* stage output and the EXT SLP signal from latch A6U39B. The Exclusive-Or gate supplies the drive-current for the EXT IN line.

7F-20. BUFFER STAGE

The major components in the *Buffer* stage are the packaged NPN transistors (U60A through E). A6U60B and U60E drive the EXTSTATE line. The 68000 μP monitors this line for activity via the *Interrupt PAL*, A6U22. EXTSTATE is also routed to Test Connector A6J6 for in-factory test purposes. Transistors U60C,D, and A respectively provide translation and drive current for front-panel EXTERNAL ARM trigger LED. The TRGLGT signal path drives the LED..

7F-21. DIGITAL-TO-ANALOG (DAC) STAGE

The DAC circuitry converts an 8-bit 68000 μP code to an analog voltage to program the EXTERNAL ARM input amplifier trigger level. The DAC circuit is controlled by the 68000 μP. The DAC IC, A6U46, outputs a current dependent upon the 8-bit code input from the 68000 μP. This current is converted into a non-positive voltage by the first op-amp, A6U45B. Polarity switch A6U61A and op-amp A6U45A operate together to convert this non-positive output to either a positive or negative level.

The core of this circuit is the DAC IC. This CMOS device receives an 8-bit data code from the 68000 μP at pins 4 through 11 via the Data_1 data bus. Since this data bus is used for communicating with many other devices, the DAC must be strobed by the 68000 μP at the DAC EN line, pin 12, and the CTWR line at pin 13. These lines latch the valid 8-bit code into the DAC IC when they both are momentarily set low.

A6U46 receives an input current at the VREF input, pin 15. The DAC has eight internal CMOS switches that route the input current through an internal resistor ladder network either to ground, pin 2, or to the output at pin 1. The output current is dependent upon the binary code input to the eight switches. With all data lines latched HIGH, the current output at pin 1 is equal to the input current at pin 15; with all data lines set LOW, all the input current at pin 15 is shunted to ground at pin 2. There are 256 (2^8) incremental steps of signal level that can appear at the output, each step being proportional to the binary-weighted input code.

A6U45A operates in a feedback configuration to act as a current-to-voltage converter. This feedback loop keeps the output voltage of the DAC at zero Volts. Capacitor A6C56 compensates the op-amp. The input offset nulling for the op-amp loop is determined by A6R54.

Regulator A6U62, the +2.5-Volt Reference IC, sets the gain of the current-to-voltage converter loop by regulating the current supplied to the DAC at pin 15.

The voltage level at the output of A6U45B is always negative as a result of its own signal inversion. The analog CMOS switch A6U61A and op-amp A6U45A work together to convert this non-positive voltage to either a positive or negative level. The state of the TTL voltage at A6U61A pin 11 determines the polarity of the output signal at A6U45A pin 1. The TTL voltage (signal) is supplied by the 68000 µP. When this line is at a TTL HIGH, the A6U61A switch closes the contacts between pins 12 and 14, and the output of A6U46 appears at the output of A6U45A unaltered. In this case, A6U45A acts as a non-inverting buffer with resistors A6R47 and R49 setting a gain of 1.

When the 68000 µP sends a TTL LOW to the CMOS switch, the contacts between pins 13 and 14 close, and the output of A6U46 appears inverted at the output of A6U45A. The inverting action of op-amp A6U45B, results in a positive voltage with unity gain at A6U45A pin 1 output.

The reference voltage input to the DAC is +2.5 Volts. The output of the current-to-voltage converter, A6U45B, ranges from 0 to –2.5 Volts. Since the 8-bit DAC has the potential for 256 current increments, the voltage resolution of the DAC for the trigger level voltage of the EXTERNAL ARM input is about 10 millivolts. Because of this, the DAC resolution for external gate arm trigger level of the instrument is 20 mV (NOMINAL). The output voltage of buffer A6U45A ranges from –2.5 to +2.5 Volts. The trigger level voltages for the EXTERNAL ARM input for the HP 5371A is –5.0 to +5.0 Volts. The DC voltages from the DAC block are amplified in the low frequency op-amp loop of the EXTERNAL ARM Input Amp. The 68000 µP programs the DAC to output a steady DC voltage for setting EXTERNAL ARM input signal trigger levels.

7F-22. TROUBLESHOOTING PROCEDURES

EQUIPMENT NEEDED: A15 Microprocessor Extender Board, P/N 05371-60015

DMA Extender Cable, P/N 5371-60225

HP 54100A Digitizing Oscilloscope (or equivalent)

DIAGNOSTIC

The following is a list of diagnostics that can indicate a failure on the A6 assembly.

Diagnostic Test 5 Count ICs

Diagnostic Test 6 Gate Timer

Diagnostic Test 7 Measurement RAM

Diagnostic Test 20 External Amp

7F-23. BACKGROUND

The A6 DMA/Gate Assembly, P/N 05371-60018, is a multifunctional board with several interdependent functional blocks that are closely coupled with the A5 ZDT/Count Assembly. The 11 major functional blocks are:

1. DMA Input Buffers (A6U57, A6U58)
2. Control Word Latches (A6U31, A6U40)
3. PAL Decode Section (A6U16, A6U17, A6U36, A6U55)
4. DMA Address Generation Counter Chain (A6U9-A6U12, A6U28, A6U30)
5. Dump Mode Counter (A6U2B, A6U3A, A6U3C, A6U6E, A6U6F, A6U23C, A6U23DE, A6U20, A6U56C)
6. Interrupt Generation PAL (A6U22)
7. Interpolator RAM (A6U37, A6U38, A6U13, A6U14, A6U18, A6U21, A6U54)
8. ZDT Address Generation (A6U35A, A6U48)
9. System Timing Controller (A6U41, A6U32, A6U42, A6U47, A6U50, A6U59)
10. External Input Amp (A6U26, A6U43-A6U46, A6U60, A6U61)
11. Totalize Circuitry (A6U7, A6U39A, A6U53)

7F-24. A6 TROUBLESHOOTING APPROACH

The approach to troubleshooting the A6 assembly is to match the failure symptom with one of the 11 functional blocks. (See A6 Failure Symptoms.) Once the failed functional block has been identified, then the failure is isolated to the component or a group of components.

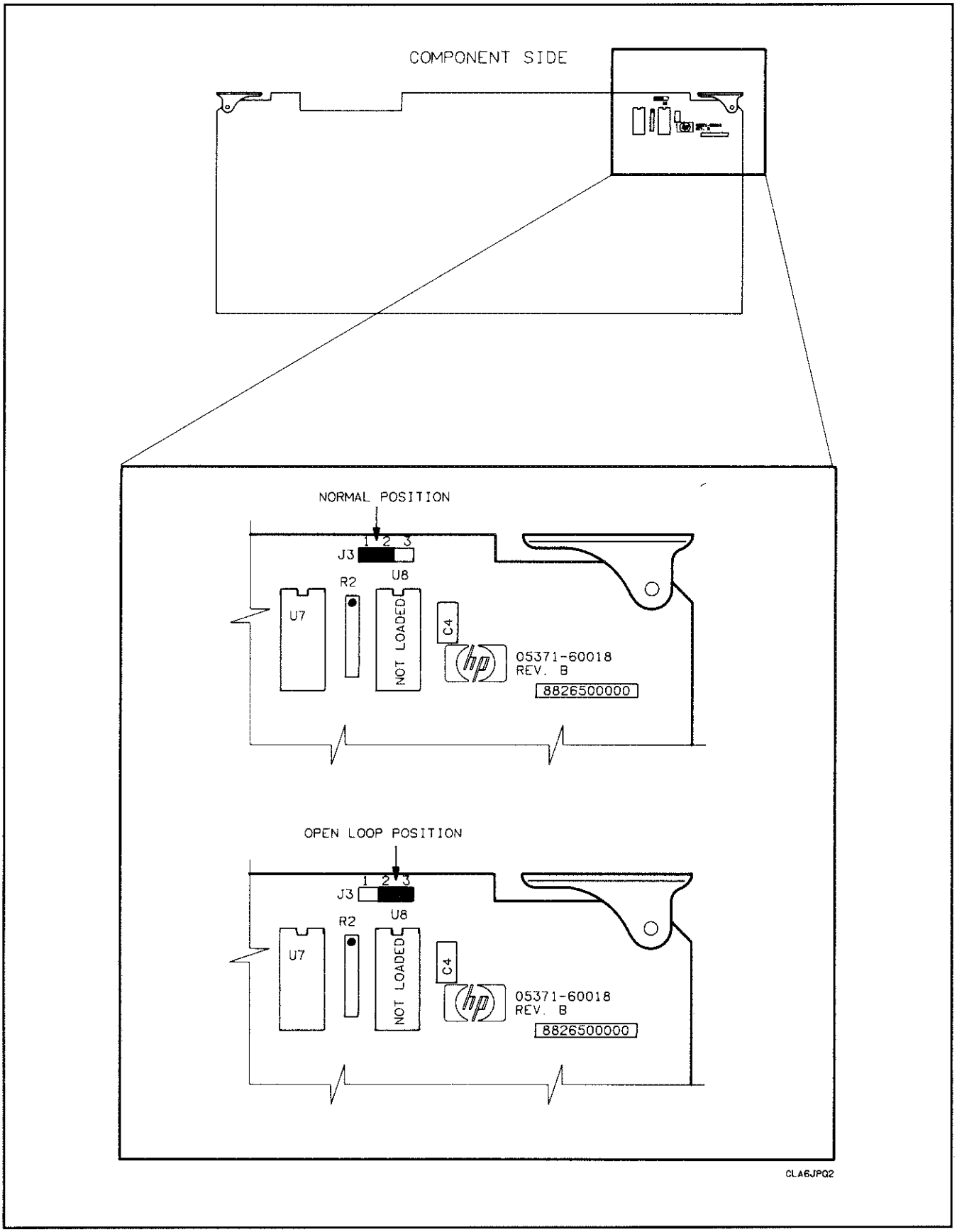


Figure 7F-2. A6 DMA/GATE Assembly Jumper Positions

7F-25. A6 FAILURE SYMPTOMS

Functional Block:	Failure Symptom:
1. DMA Inputs Buffers	HP 5371A locks up and does not function or respond to front panel.
2. Control Word Latches	HP 5371A miscounts and/or never completes a measurement
3. PAL Decode Section	HP 5371A miscounts and Diagnostics 5 and 7 fail.
4. DMA Address Generation Counter Chain	HP 5371A miscounts and Diagnostics 7 fails all the Measurement RAM and/or all the Interpolator RAMs.
5. Dump Mode Counter	HP 5371A HP-IB dump mode does not function.
6. Interrupt Generation PAL	HP 5371A display never gets updated(frozen).
7. Interpolator RAMs	HP 5371A Diagnostic 7 fails the Interpolator RAMs
8. ZDT Address Generation	HP 5371A does not function and incorrect results are given. Diagnostics 5 and 7 pass.
9. System Timing Controller	HP 5371A Diagnostic Test 6 fails.
10. External Input Amp	HP 5371A External Input Amp does not function properly.
11. Totalize Circuitry	HP 5371A Totalize function does not operate properly.

7F-26. A6 TROUBLESHOOTING PREPARATION

Place the A6 assembly, P/N 05371-60018, on the A15 Microprocessor Extender Board, P/N 05371-60015. Use the DMA Extender Cable, P/N 05371-60225, to connect the A6 assembly to the A5 assembly. Move jumper A6W1 to its open loop position. (See *Figure 7F-2.*) Connect the frequency standard output at the rear panel to channel A. Turn the HP 5371A from STANDBY to ON. After the power-up sequence (ignore any failure messages), press the front panel PRESET hardkey.

7F-27. A6 TROUBLESHOOTING PROCEDURES

A. DMA Input Buffers Troubleshooting

1. Replace A6U57 and/or A6U58 if they are not at the levels as indicated in *Figure 7F-3*.

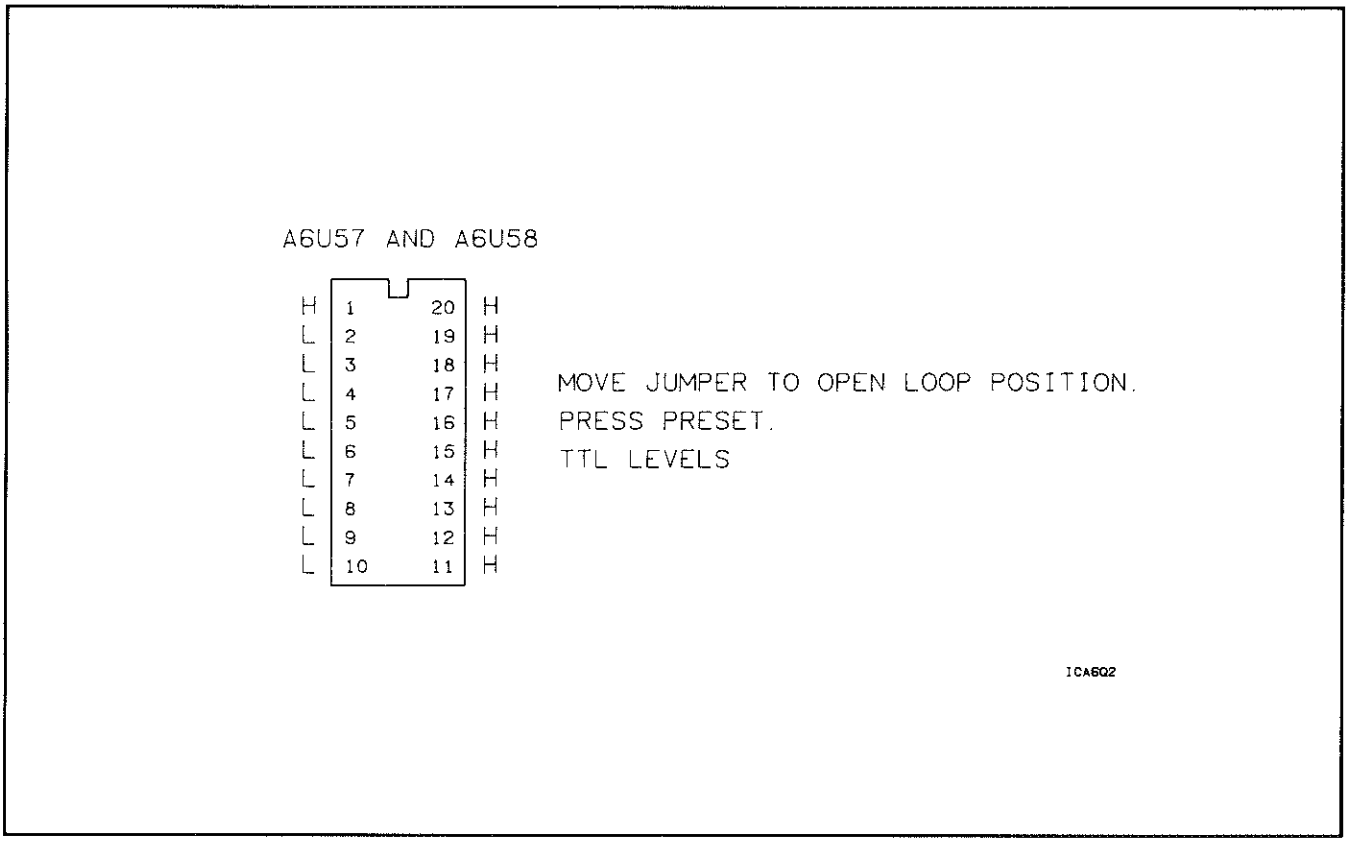


Figure 7F-3. A6U57 and A6U58 Signal Levels

B. Control Word Latches

With the board or counter configuration as specified, check the following IC pins for the levels indicated:

1. A6U40(12): Jumper Position = Open Loop, Timebase Out to Channel A.
   Press PRESET and check for TTL Low
   Change measurement to Continuous Time Interval, check for TTL High

2. A6U40(13): Jumper Position = Open Loop, Timebase Out to Channel A.
   Press PRESET and check for TTL High
   Change measurement to Totalize, arming to Manual, Check for TTL Low

3. A6U40(14): Jumper Position = Open Loop, Timebase Out to Channel A
   Press PRESET and check for TTL High
   Change measurement to Continuous Time Interval and check for TTL Low

4. A6U40(15): Jumper Position = Open Loop, Remove Timebase Out to Channel A
   Press SINGLE/REPET key, SINGLE Light should be ON
   Press PRESET, GATE Light should be ON and A6U40(15) is TTL Low
   Press RESTART and Hold, check for TTL High

5. A6U40(16): Jumper Position = Normal, Timebase Out to Channel A
Press PRESET and check for TTL Low
Press SYSTEM, change Result Format field to "Binary", change Addressing Field to "TALK ONLY", change Print field to "MEAS RESULT",
Press RESTART (GATE Light ON) check for TTL High (may toggle Low momentarily)

6. A6U40(17): Jumper Position = Normal, Timebase Out to Channel A
Press PRESET and check for TTL High
Change measurement to Frequency check for TTL Low

7. A6U40(18): Jumper Position = Normal, Timebase Out to Channel A
Press SYSTEM, change Result Format field to "Binary",
Press FUNCTION and check for TTL Low
Change measurement to Frequency and check for TTL High

8. A6U40(19): Always TTL Low

9. A6U31(16): Jumper Position = Open Loop, Timebase Out to Channel A
Press PRESET and check for TTL Low

10. A6U31(18): Jumper Position = Open Loop, Timebase Out to Channel A
Press PRESET and check for TTL Low
Change measurement to Continuous Time Interval, check for TTL High

11. A6U31(19): Jumper Position = Open Loop, Timebase Out to Channel A
Press PRESET and check for TTL Low

C. PAL Decode Section

1. A6U17(12-18) & A6U55(13):
Jumper Position = Normal, Timebase Out to Channel A
Press SINGLE/REPET key,
Remove Channel A input (GATE Light OFF) and check for TTL High
Press RESTART (GATE Light ON) and check for TTL Low

2. A6U17(19): Jumper Position = Normal, check that pin 19 is always TTL High

3. A6U16 and A6U36: Jumper Position = Open Loop, Remove TBO to Channel A Persistence = 1 second (on HP 54100A Oscilloscope) (See Table Below)

GATE Light Off (Press RESTART and Hold)	GATE Light ON (Press RESTART)
A6U31(1-7) is TTL High	A6U31(1-7) is Active
A6U31(8-11) is TTL Low	A6U31(8-11) is TTL Low
A6U31(12-19) is TTL High	A6U31(12-19) is Active
A6U16(1-9,11-20) is TTL High	A6U16(1-5,7-9,11-17) is Active
A6U16(10) is TTL Low	A6U16(6,18,19,20) is TTL High
	A6U16(20) is TTL High

D. DMA Address Generation Counter Chain

1. Jumper Position = Open Loop, Timebase Out to Channel A
Press PRESET

2. Observe A6U10(3). Should appear as in *Figure 7F-4*. A6U10(2) is twice the period of A6U10(3). A6U10(6) is twice the period of A6U10(2). A6U10(7) is twice the period of A6U10(6).

3. Observe A6U9(3). Should appear as in *Figure 7F-4*. A6U9(2) is twice the period of A6U9(3). A6U9(6) is twice the period of A6U9(2). A6U9(7) is twice the period of A6U9(6).

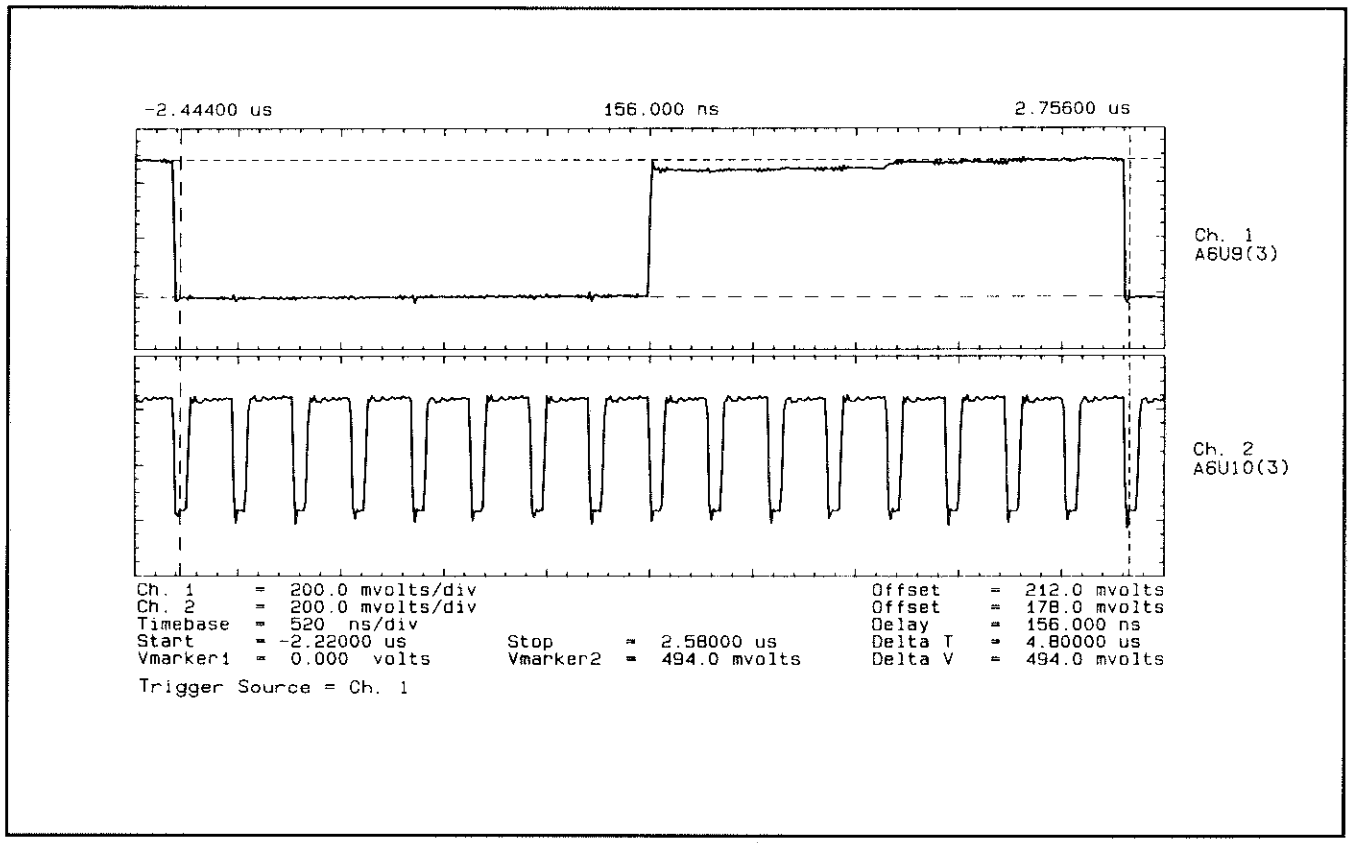


Figure 7F-4. A6U10(3) Waveform

4. Observe A6U11(3). Should appear as in *Figure 7F-5*. A6U11(2) is twice the period of A6U11(3). A6U11(6) is twice the period of A6U11(2). A6U11(7) is twice the period of A6U11(6).

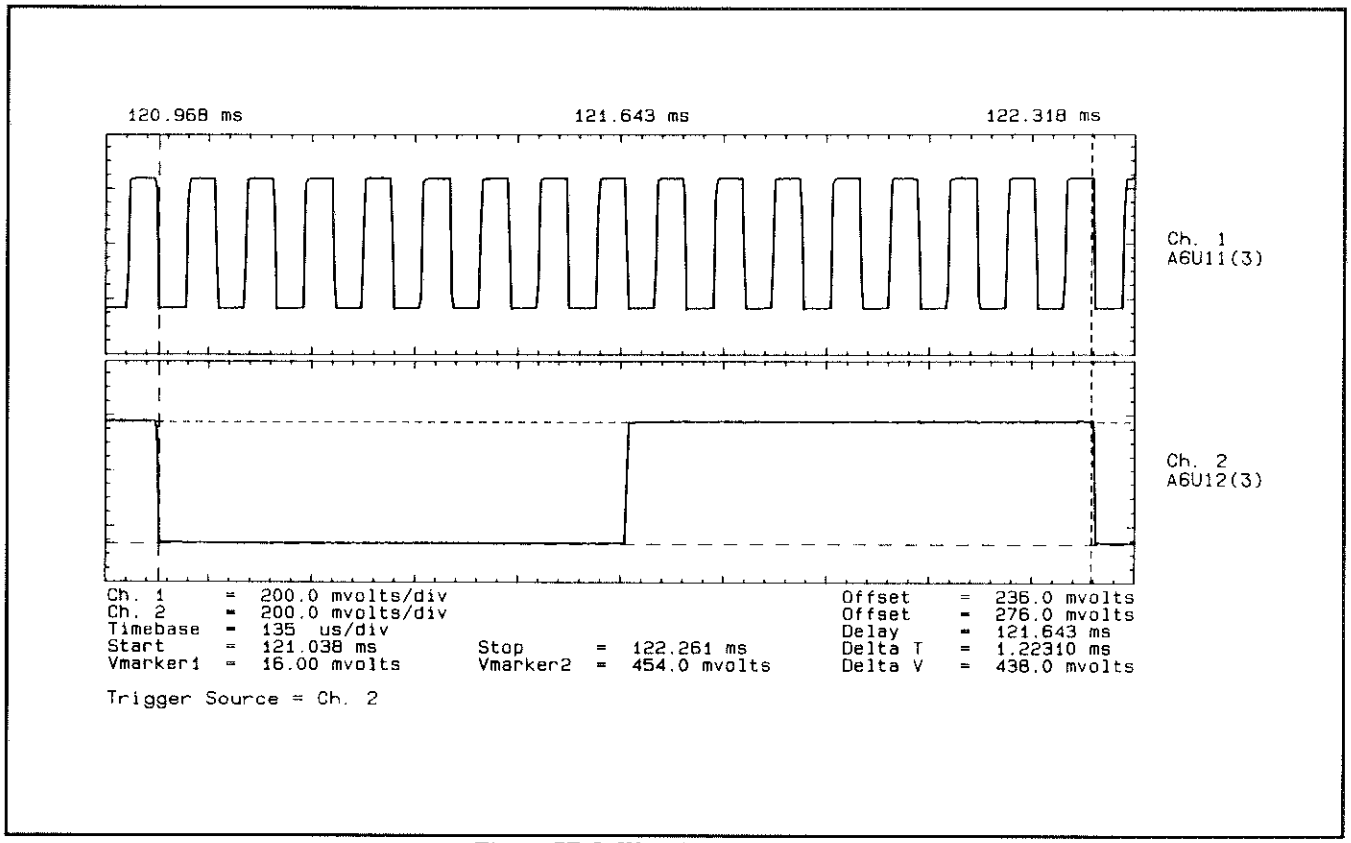


Figure 7F-5. Waveforms at A6U11(3)

E. Dump Mode Counter

1. Jumper Position = Open Loop, Timebase Out to Channel A
   Press SYSTEM
   Address Field = TALK ONLY
   Print Field = MEAS
   RESULT Result Format Field = BINARY
   Check that A6U20(1-3,5,8,12,15) is TTL Low.
   Check that A6U20(4,6,7,9,10,11,13,14,16) is TTL High.

F. Interrupt Generation PAL

1. Jumper Position = Open Loop, Timebase Out to Channel A
   Press PRESET
   Persistence = Infinite (on HP54100 Oscilloscope)
   Observe A6U22 with oscilloscope. (See table below.)

GATE Light Off (Press RESTART and Hold)	GATE Light ON (Press RESTART)
A6U22(1,5,9) is TTL Low	A6U22(1,9) is TTL Low
A6U22(2,7,11,12) is TTL High	A6U22(2,5,7,12) is Active
	A6U22(11) is TTL High (may go low momentarily)

G. Interpolator RAMs

1. Jumper Position = Normal, Timebase Out to Channel A

Press TEST, then run diagnostic test #7, Measurement RAM.

With oscilloscope, observe signals at A6U37(11,13,16,18) and A6U38(11,13,16,18). (See *Figure 7F-6*).

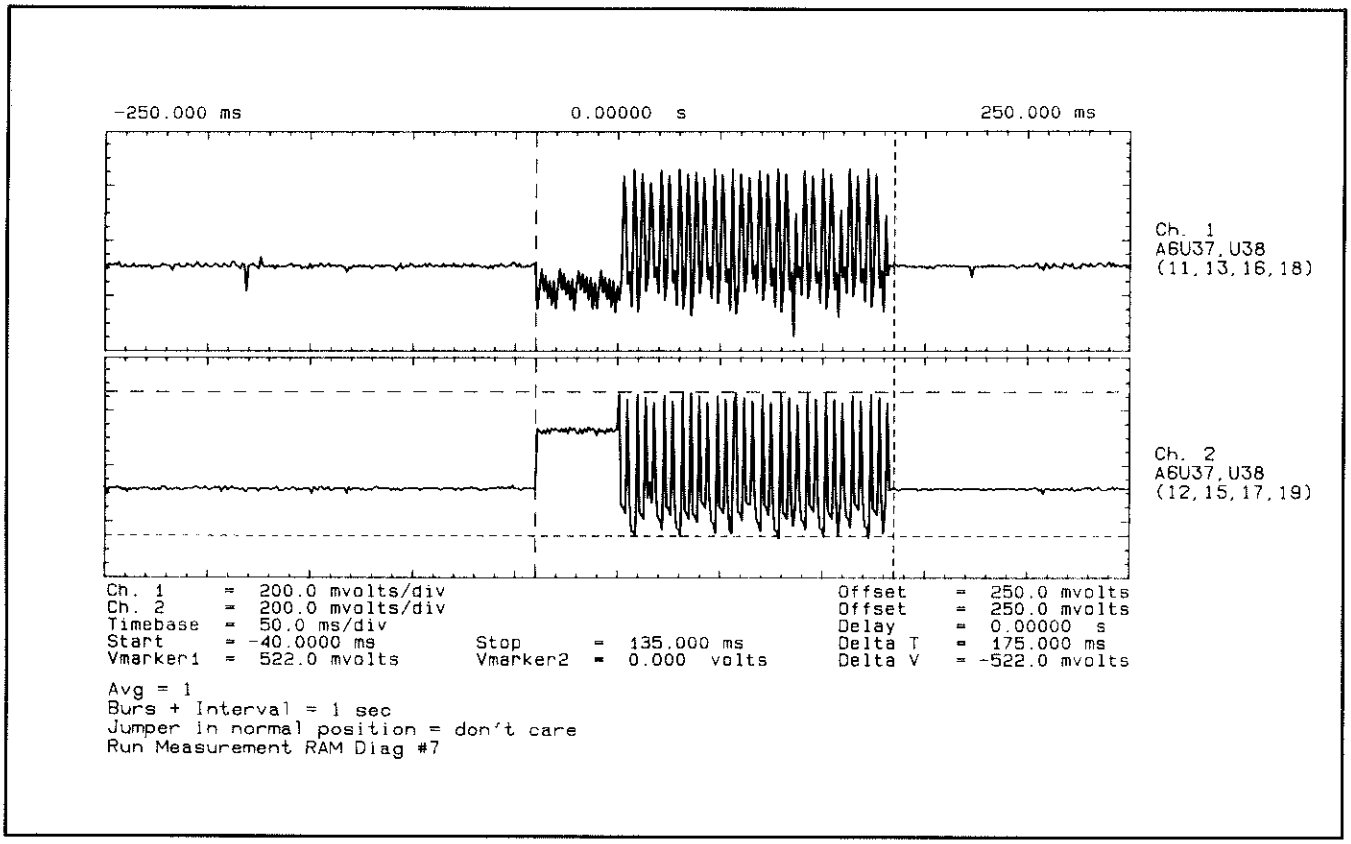


Figure 7F-6. Waveforms at A6U37 and A6U38

2. Detach DMA Extender Cable, P/N 05371-60225, from the A6 assembly. Observe signals at A6U13(11-18) and A6U18(11-18). (See *Figure 7F-7.*)

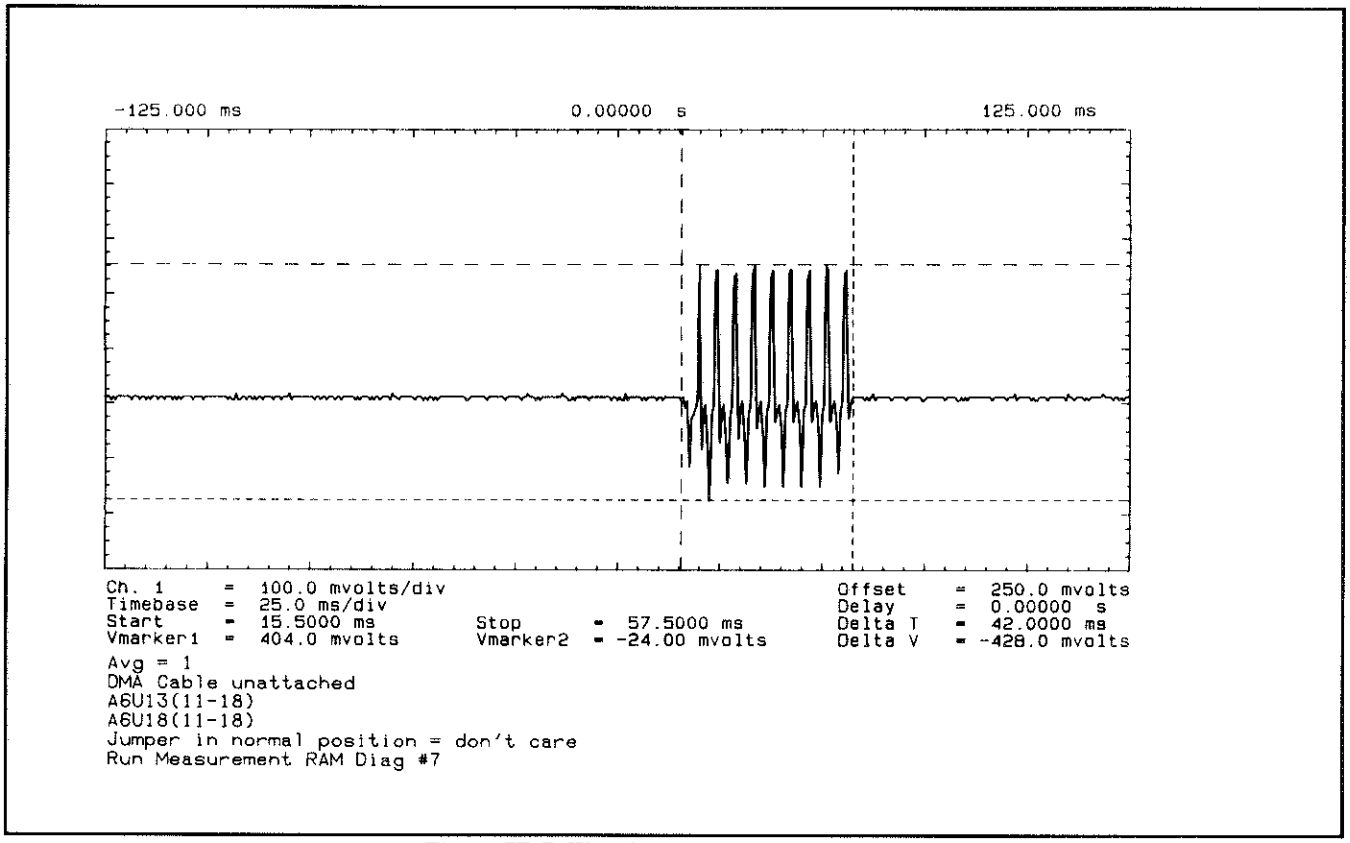


Figure 7F-7. Waveforms at A6U13 and A6U18

3. Re-attach DMA Extender Cable to the A6 Assembly. Change the jumper to the open loop position.

   Check A6U21(2,3,5,6) for a TTL Low. Press RESTART and Hold (GATE Light OFF), check that A6U21(2,3,5,6) are TTL High.

   Press RESTART and Hold (GATE Light OFF) Check that A6U14(2,3,5,6) are TTL Low, check that A6U14(4) is TTL High.

   Press PRESET, Check that A6U14(2,5,6) are TTL Low, check that A6U14(3,4) are as shown in *Figure 7F-8.*

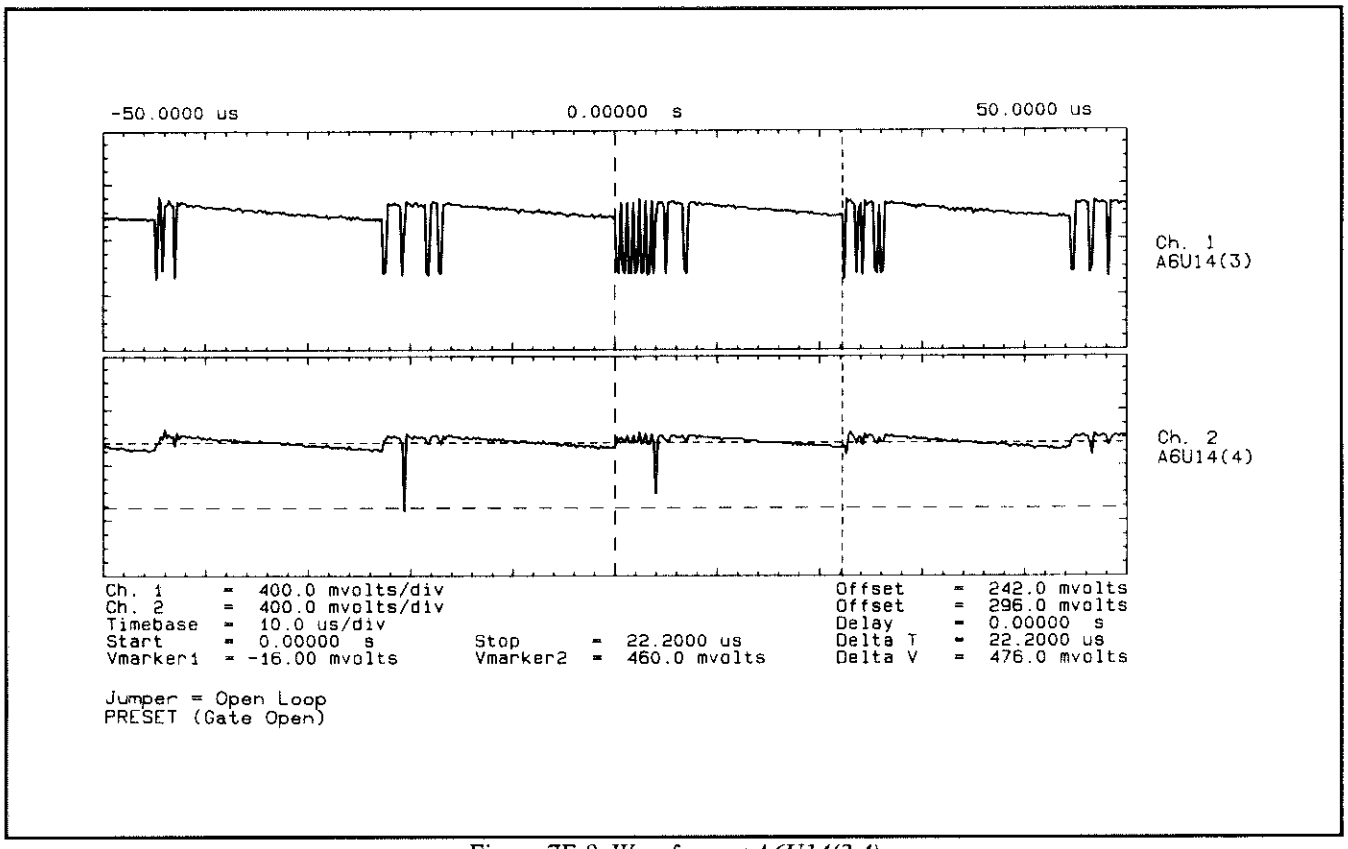


Figure 7F-8. Waveform at A6U14(3,4)

H. ZDT Address Generation

1. Jumper Position = Open Loop, Timebase Out to Channel A

2. Press PRESET. Check that A6U48(4,7,9) are as shown in *Figure 7F-9.*
   Check that A6U42(3,6,10) are TTL High.
   Press RESTART and Hold (GATE Light OFF).
   Check that A6U48(4) is mostly TTL High (Momentarily goes Low)

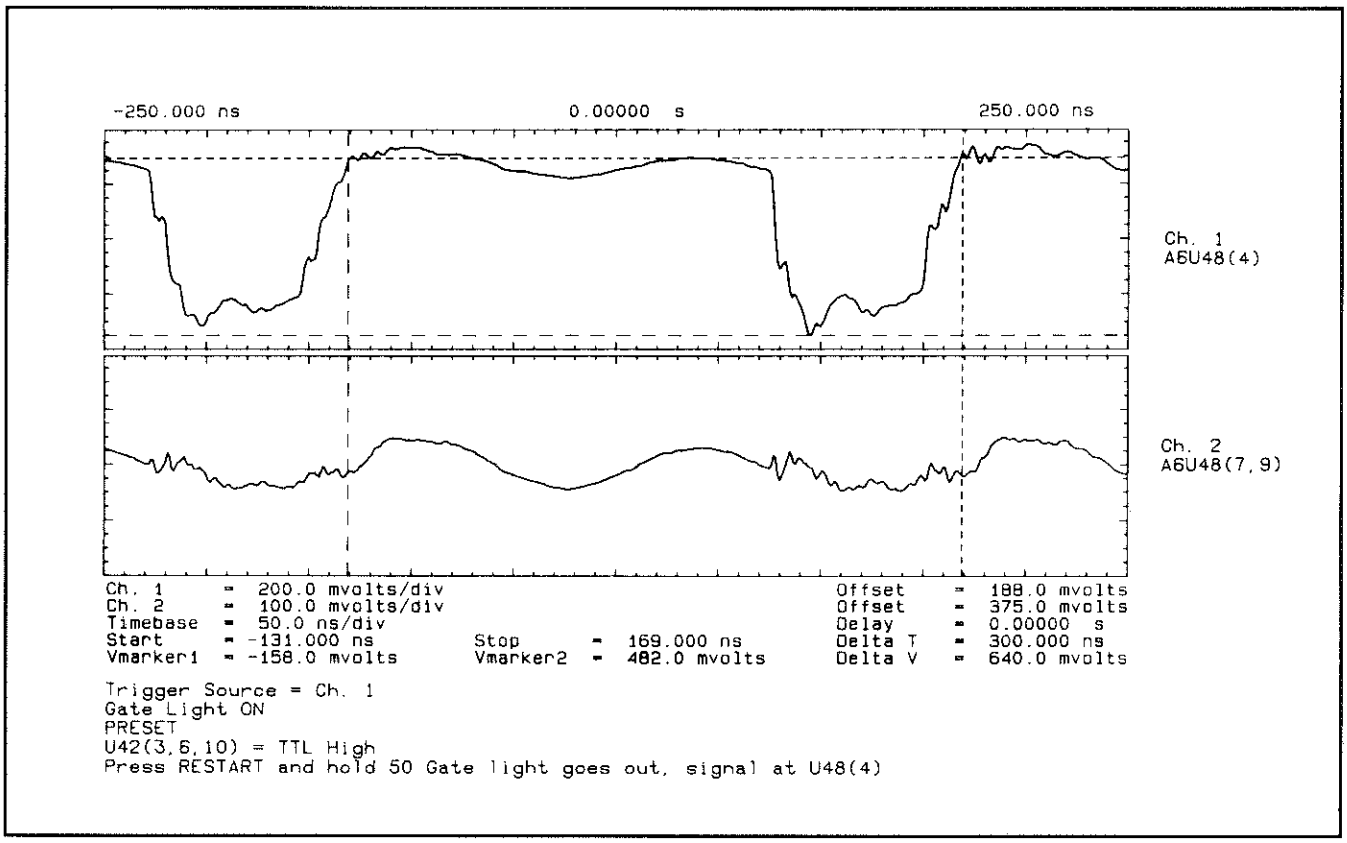


Figure 7F-9. Waveforms at A6U48(4,7,9)

3. Press PRESET. A6U35(2,3) is as shown in *Figure 7F-10*. A6U35(1) is TTL Low. Press RESTART and Hold. A6U35(1) is TTL High.

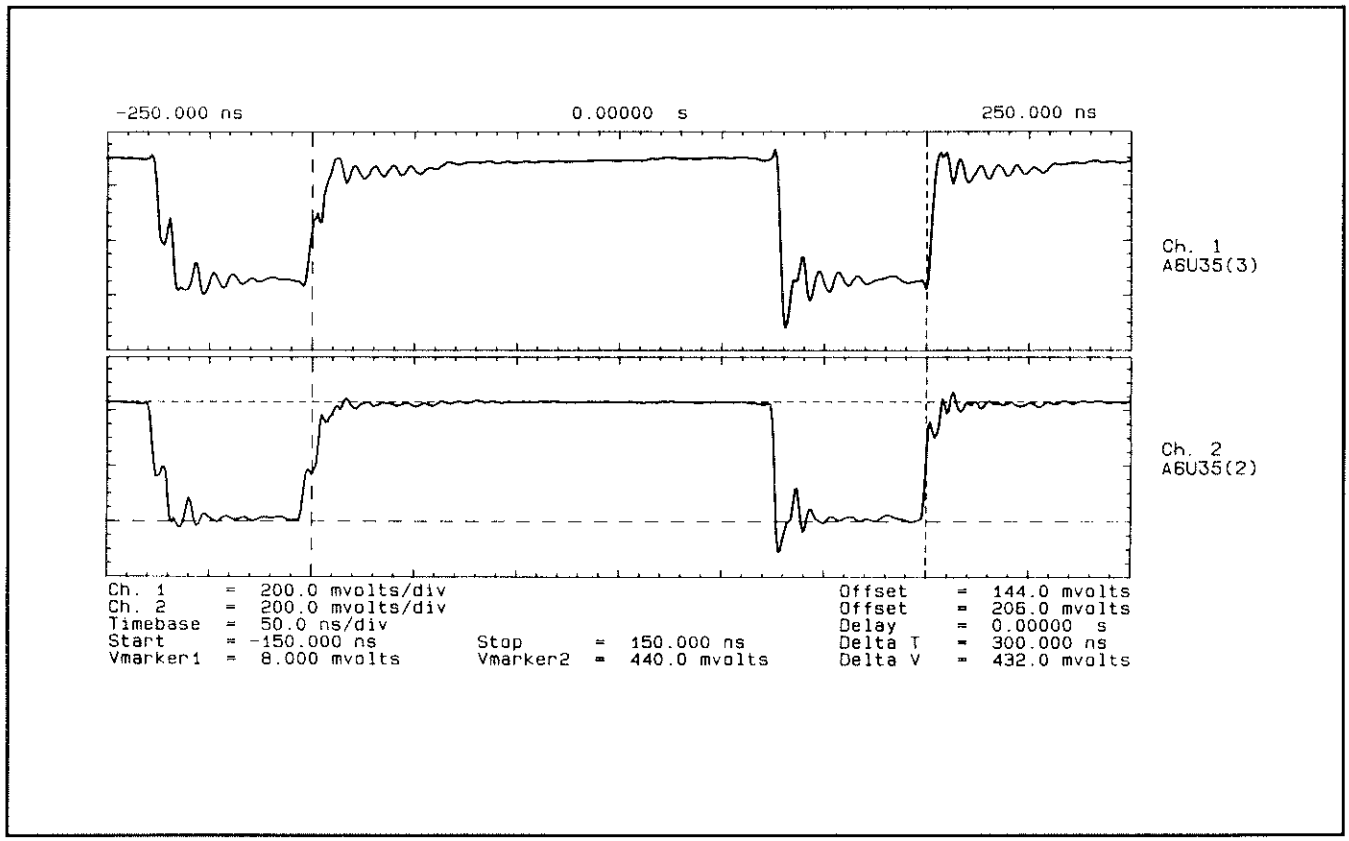


Figure 7F-10. Waveforms at A6U35(2,3)

I. System Timing Controller

1. Jumper Position = Normal, Timebase Out to Channel A

2. Press PRESET. A6U41(7) & A6U59(9) are as shown in *Figure 7F-11*.

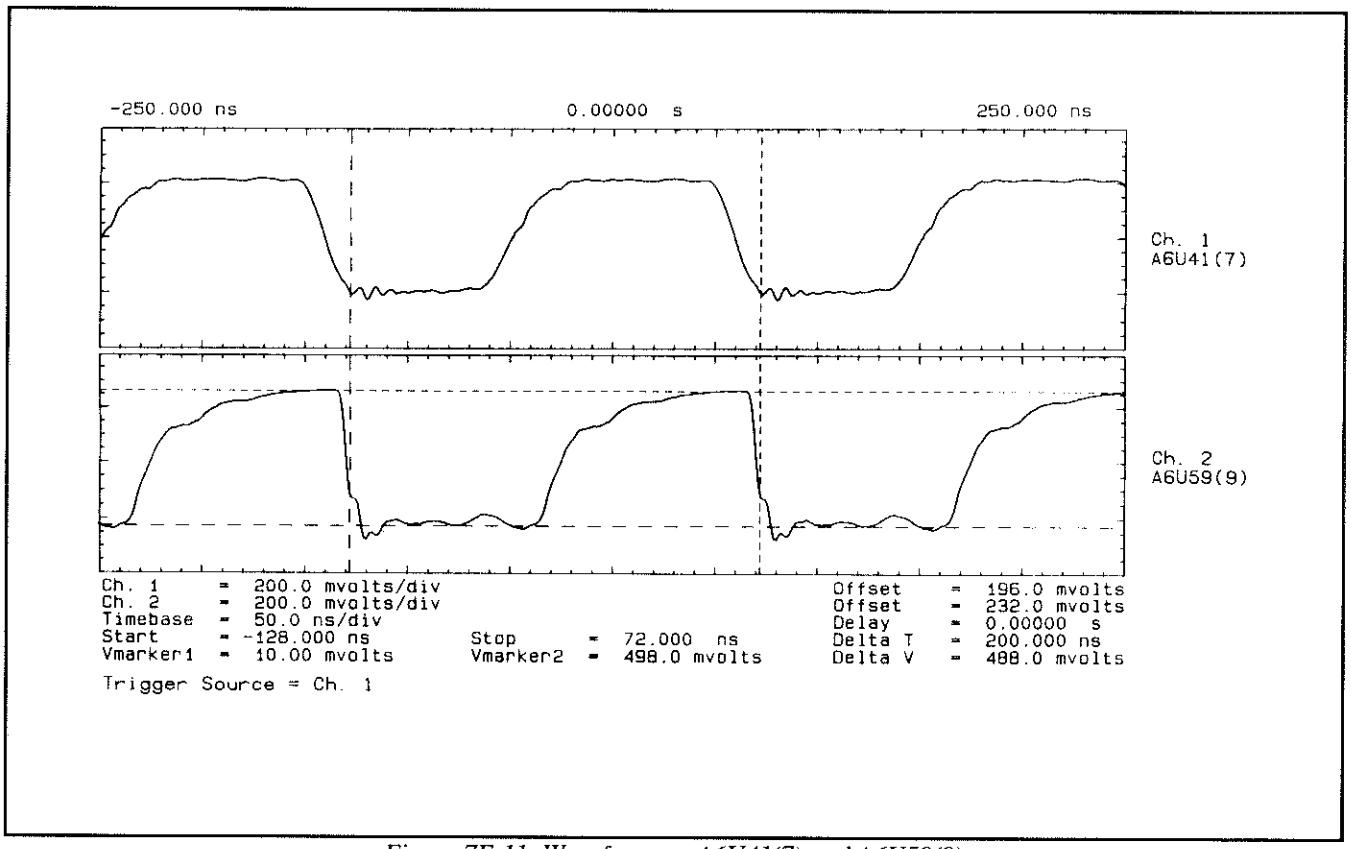


Figure 7F-11. Waveforms at A6U41(7) and A6U59(9)

3. Change arming to Interval Sampling. Press RESTART. A6U41(2,4) are as shown in *Figure 7F-12*. Change arming to Automatic. Check that A6U41(2,4) are as shown in *Figure 7F-13*.

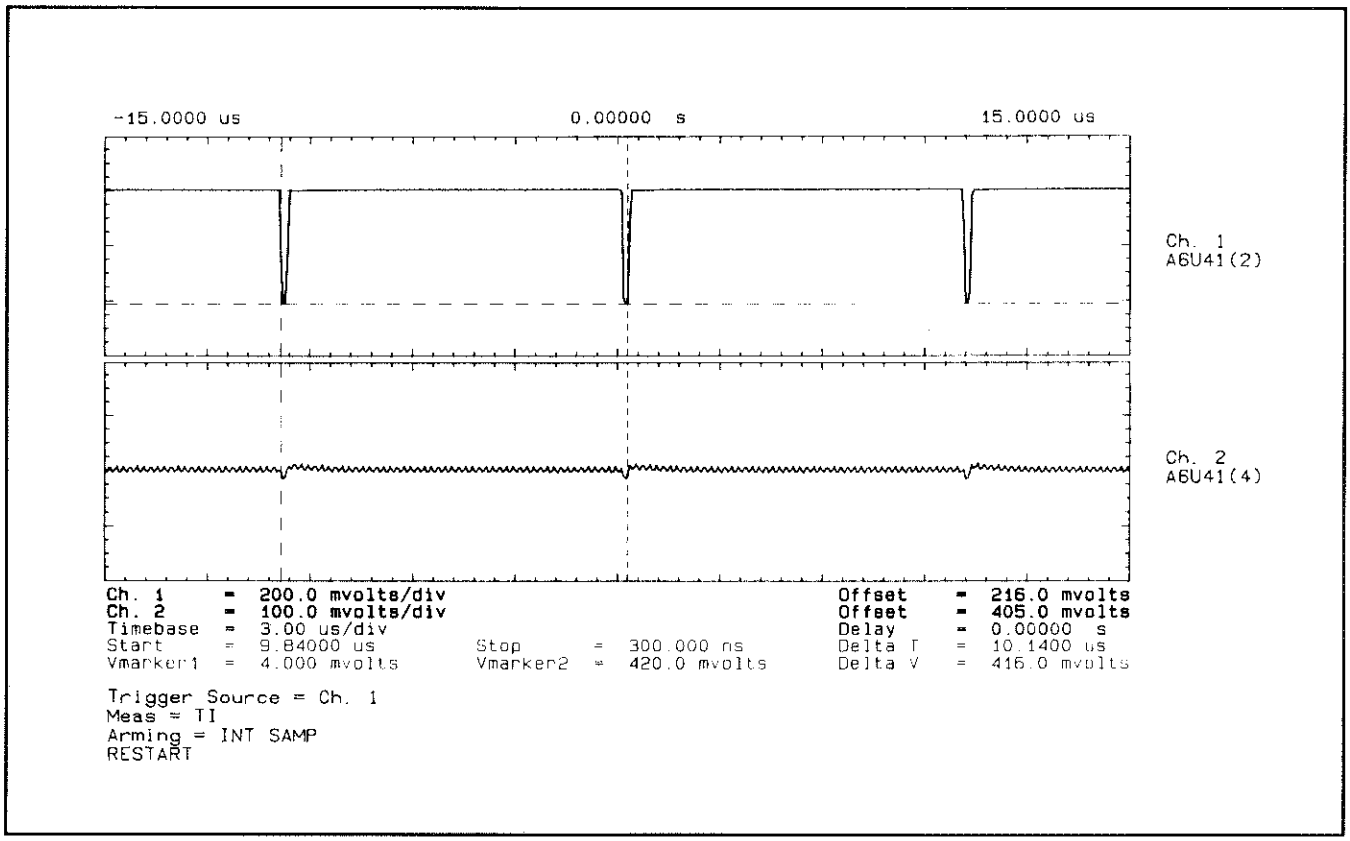


Figure 7F-12. Waveforms at A6U41(2,4)

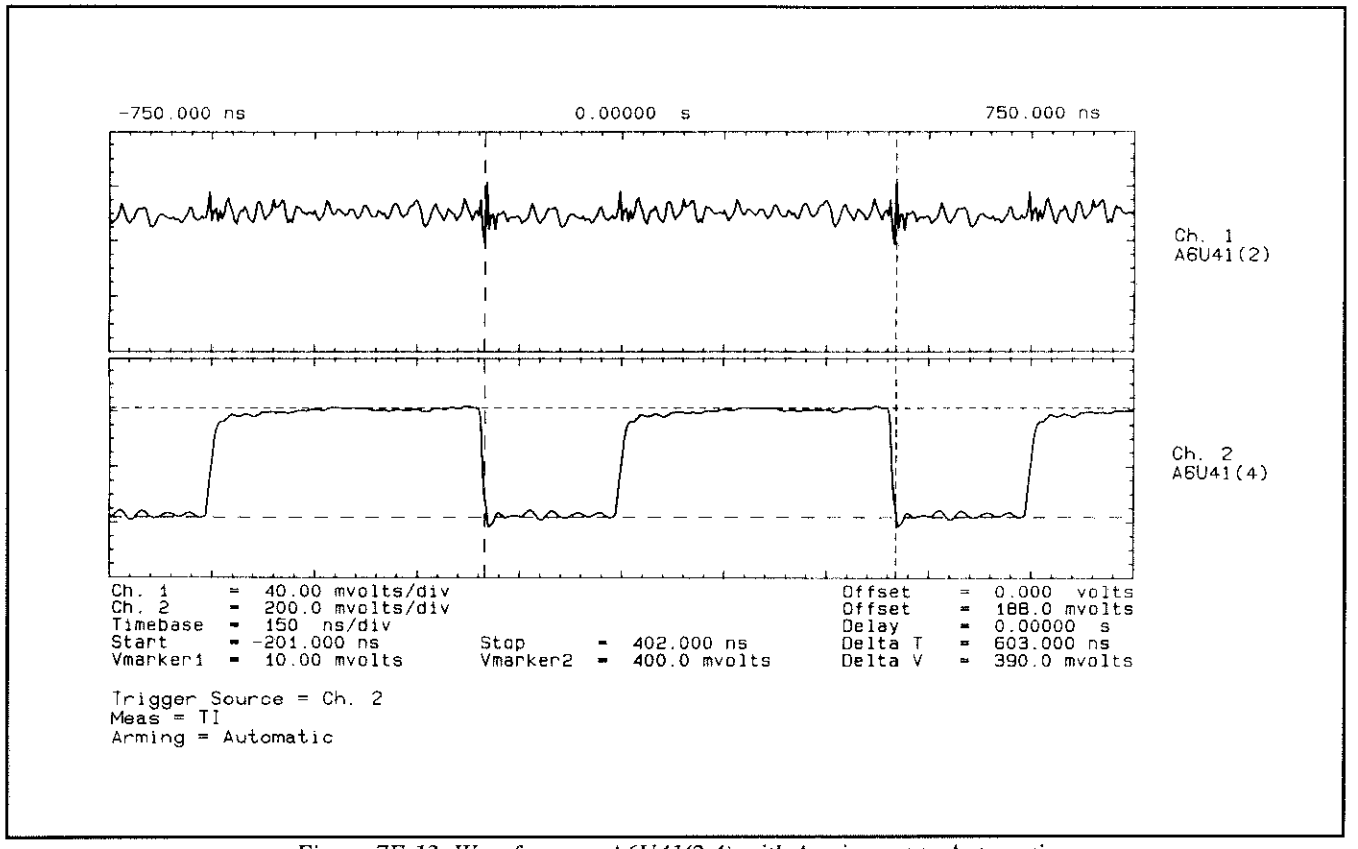


Figure 7F-13. Waveforms at A6U41(2,4) with Arming set to Automatic

4. Press PRESET. Check that A6U32(5,9) are as shown in *Figure 7F-14*. Check that A6U42(5,9) are as shown in *Figure 7F-15*. Check that A6U50(3,4) are as shown in *Figure 7F-16*.

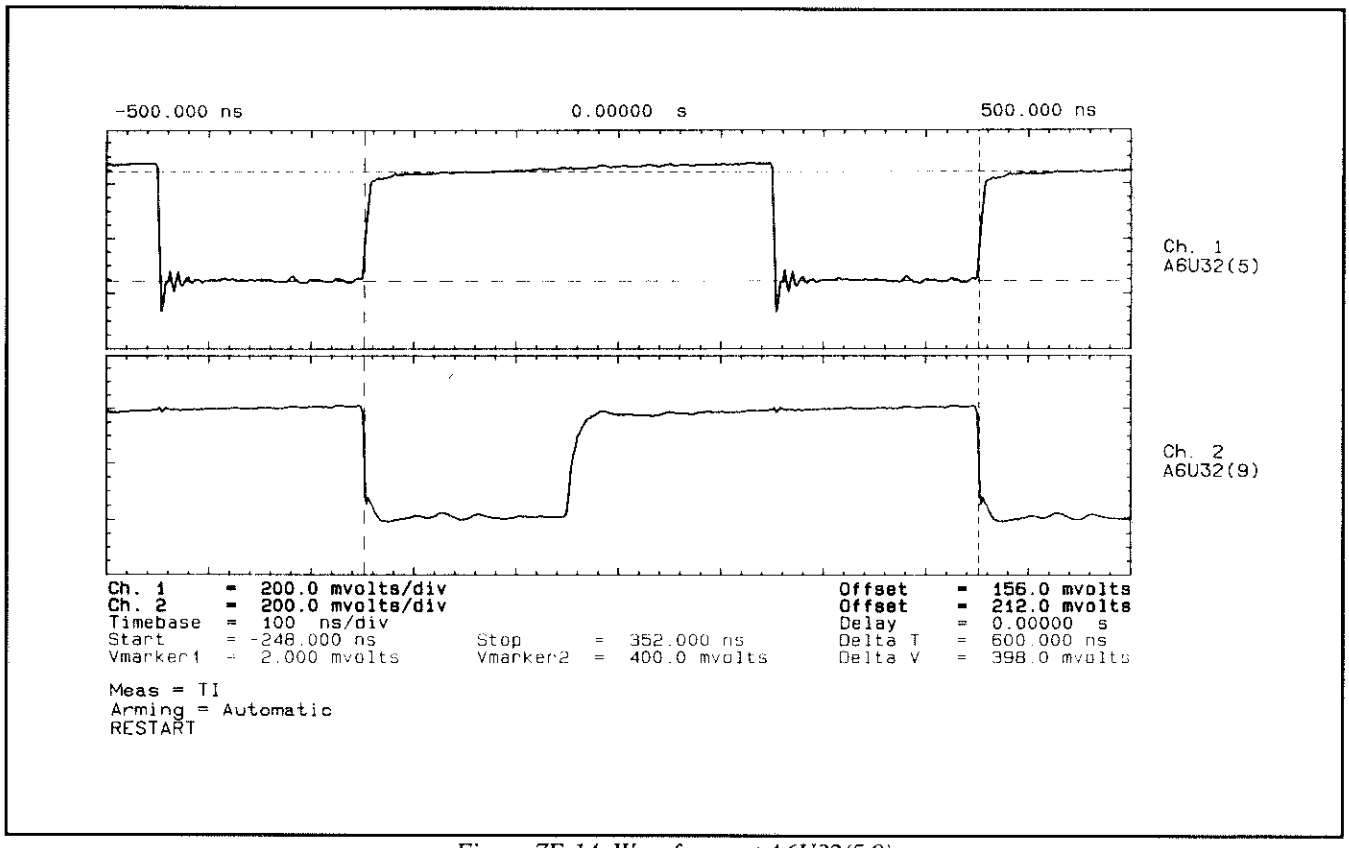


Figure 7F-14. Waveforms at A6U32(5,9)

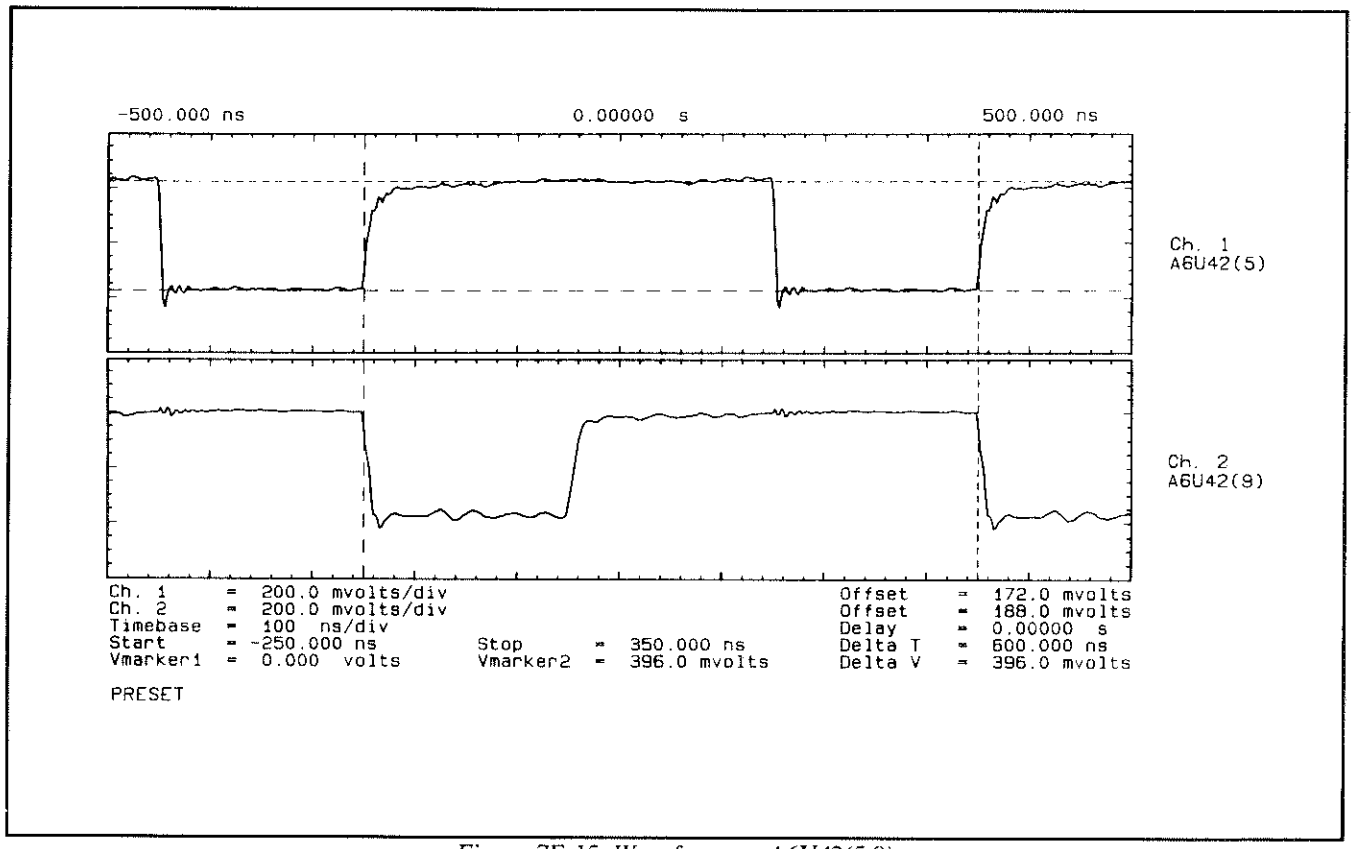


Figure 7F-15. Waveforms at A6U42(5,9)

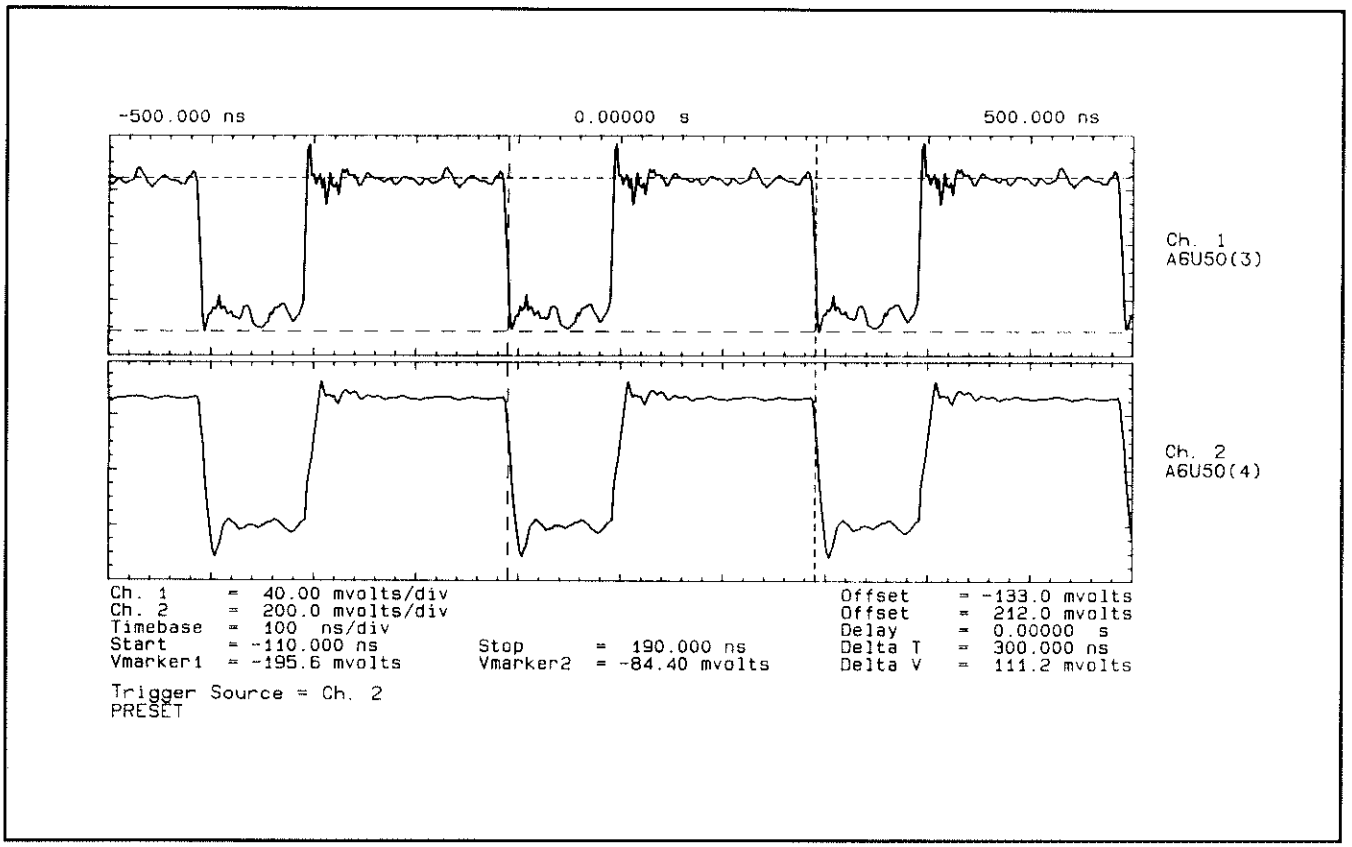


Figure 7F-16. Waveforms at A6U50(3,4)

5. Change arming to Interval Sampling. Check that A6U47(14,15) is as shown *Figure 7F-17.*

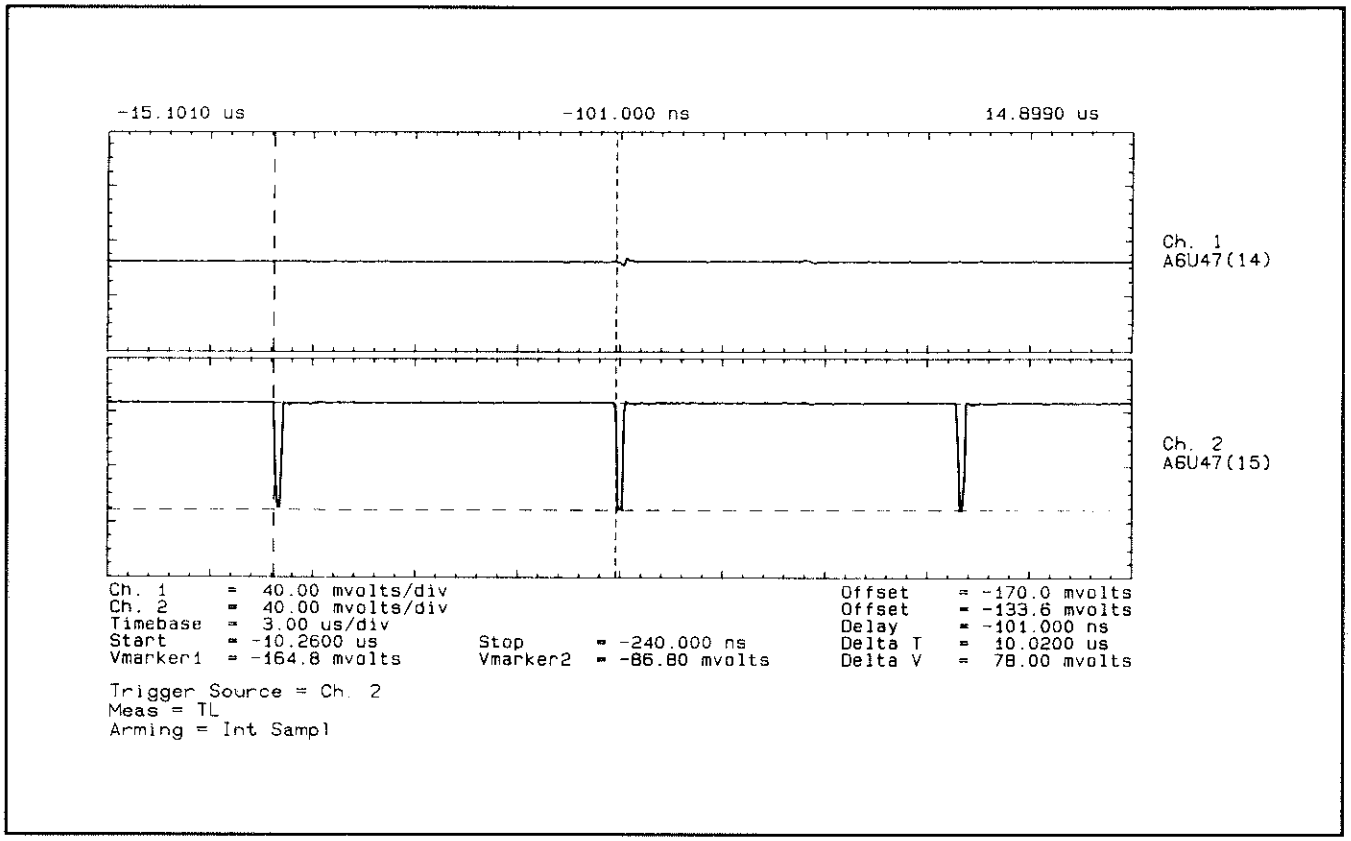


Figure 7F-17. Waveforms at A6U47(14,15)

A. External Arm Input

1. Jumper Position = Normal, Timebase Out to Channel A

2. Verify 2.5 volts at TP2, A6U62(2). Replace, if not present.

3. Press INPUT key. Move cursor to "External Arm Level" field. Monitor TP1, A6U45(1), with a DVM. Vary "External Arm Level" Field as indicated below:

External Arm Level (Volts)	DVM Reading (Volts)
–5.00	–2.25 ±.05
–4.00	–1.80 ±.05
–3.00	–1.35 ±.05
–2.00	–0.90 ±.05
–1.00	–0.45 ±.05
0	0 ±.05
+1.00	+0.45 ±.05
+2.00	+0.90 ±.05
+3.00	+1.35 ±.05
+4.00	+1.80 ±.05
+5.00	+2.25 ±.05

If readings are not correct, trace failure back to A6U46, DAC.

4. Return "External Arm Level" field to 0 volts. Verify EXT INPUT signal output at A6U44(3). (See *Figure 7F-18.*) If not present, trace failure back to A6J3.

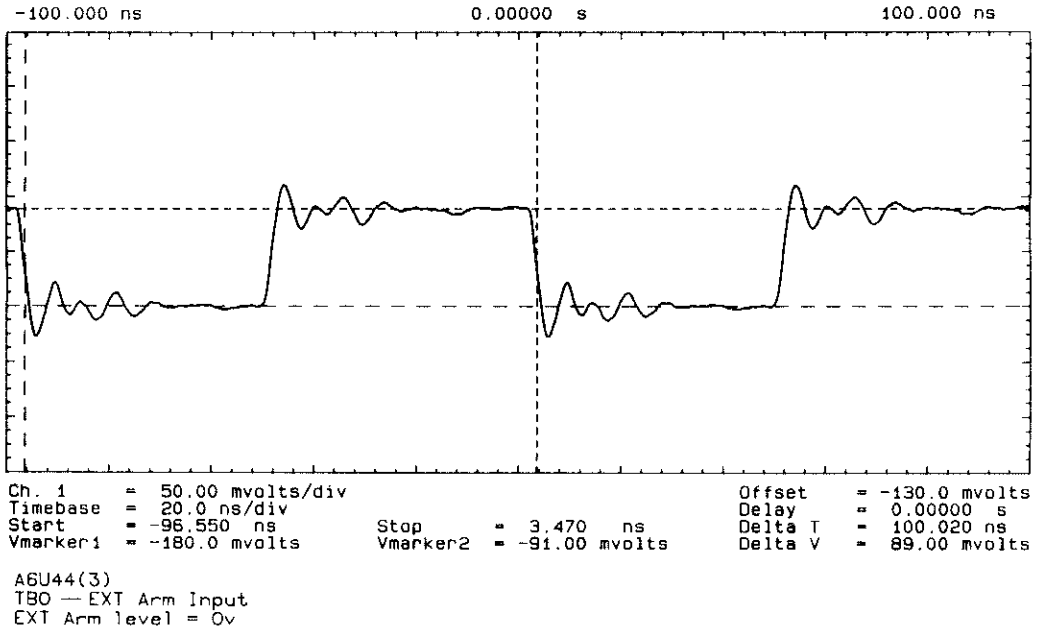


Figure 7F-18. Waveforms at A6U44(3)

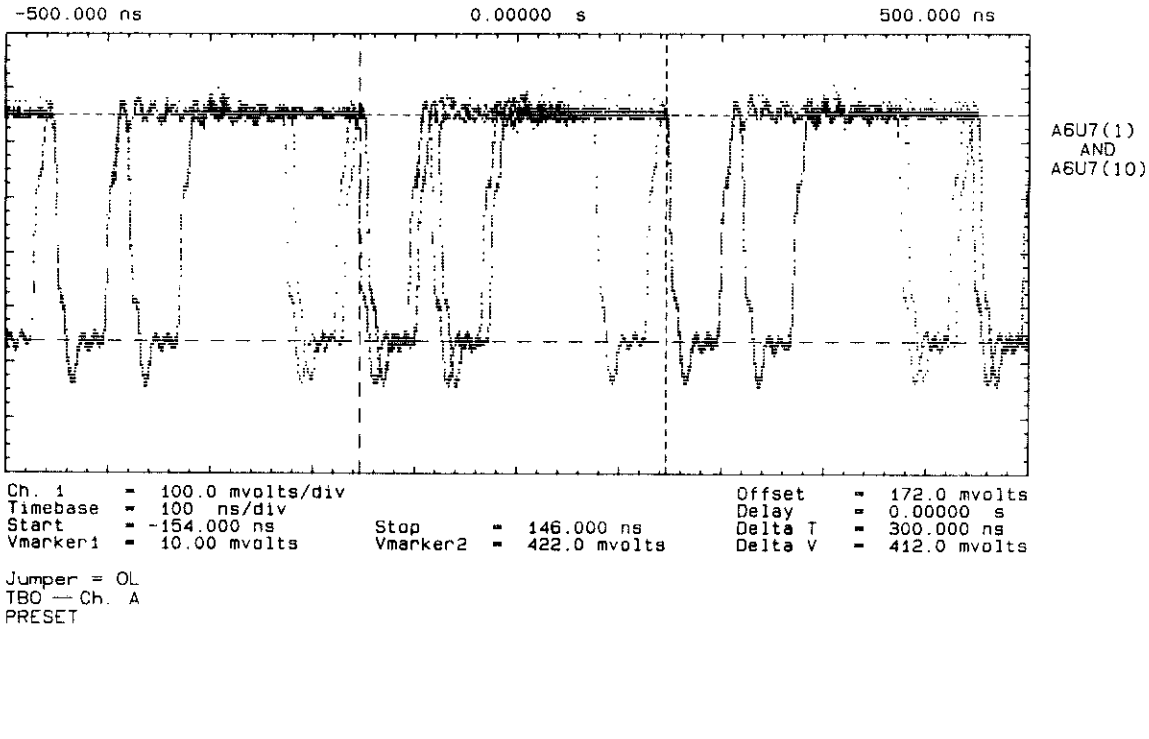


Figure 7F-19. Waveforms at A6U7(1,10)

A. Totalize

1. Jumper Position = Open Loop, Timebase Out to Channel A Press PRESET. Observe that signals at A6U7(1,10) are as shown in *Figure 7F-19*. Change measurement to Totalize. Observe that signals at A6U7(1,10) are as shown in *Figure 7F-20*.

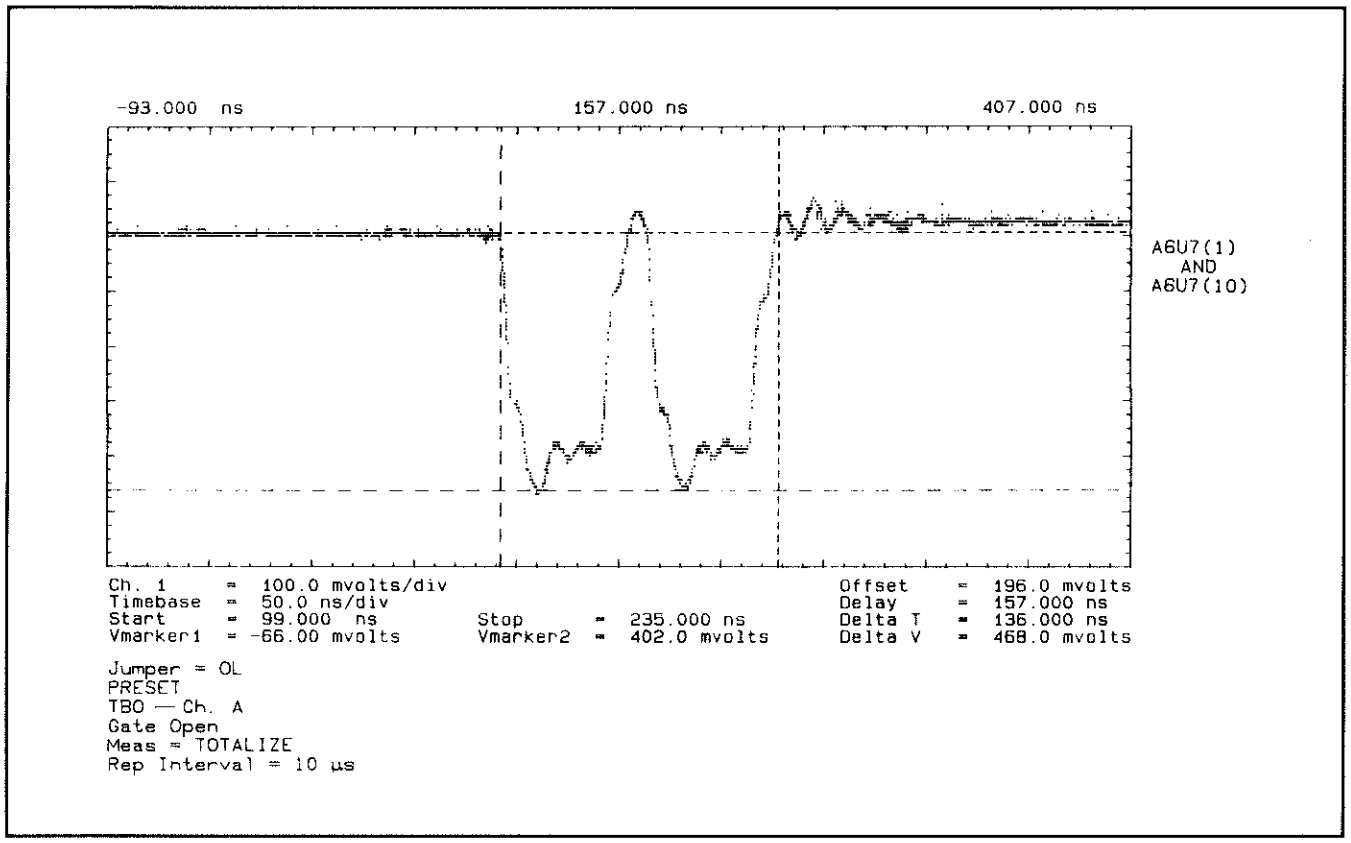


Figure 7F-20. Waveforms at A6U7(1,10) in Totalize Mode

2. Jumper Position = Open Loop, Timebase Out to Channel A Press PRESET. Observe signals at A6U53(5,13), see *Figure 7F-21*. Change measurement to Totalize. Observe signals at A6U53(5,13), see *Figure 7F-22*. (Rep Int=10uSec)

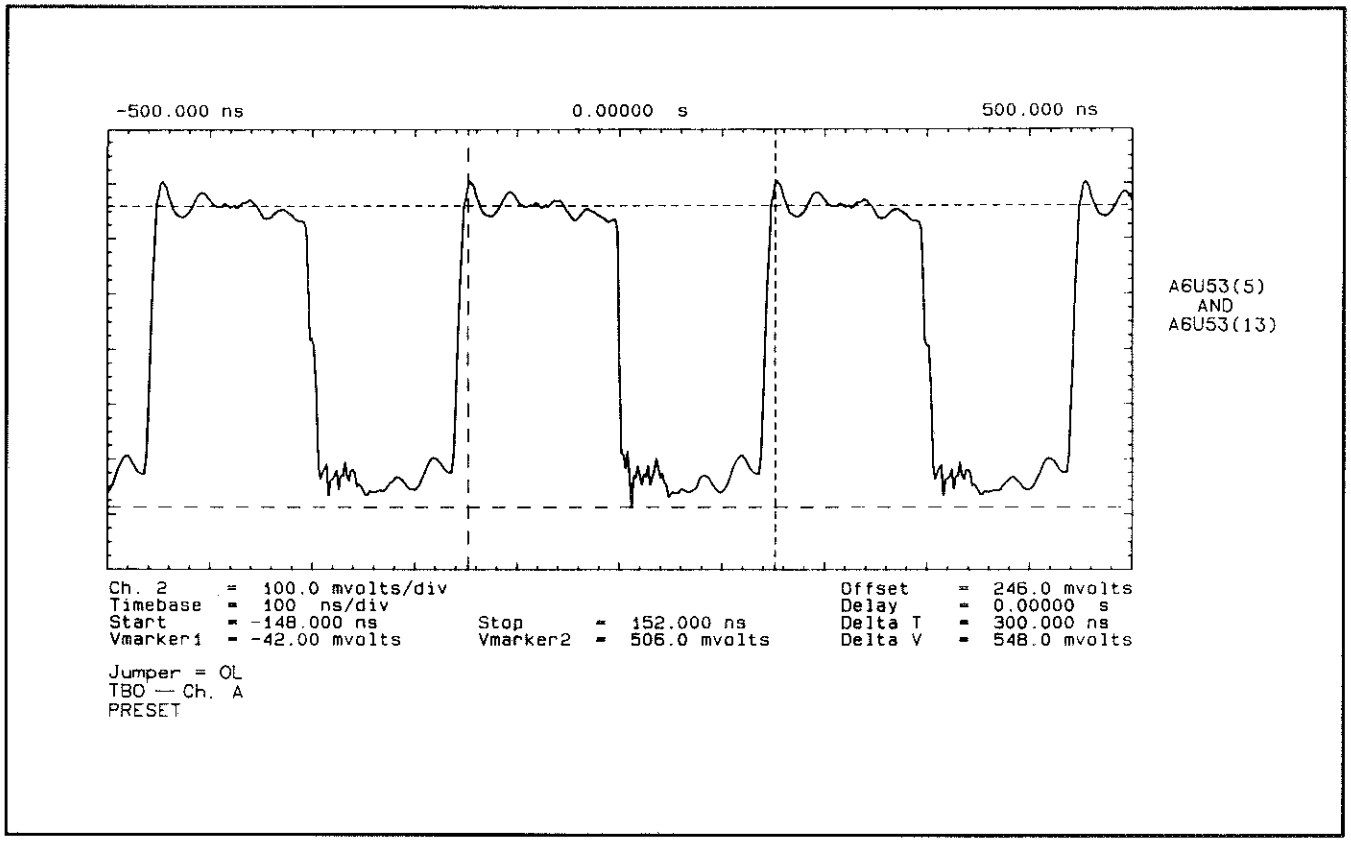


Figure 7F-21. Waveforms at A6U53(5,13)

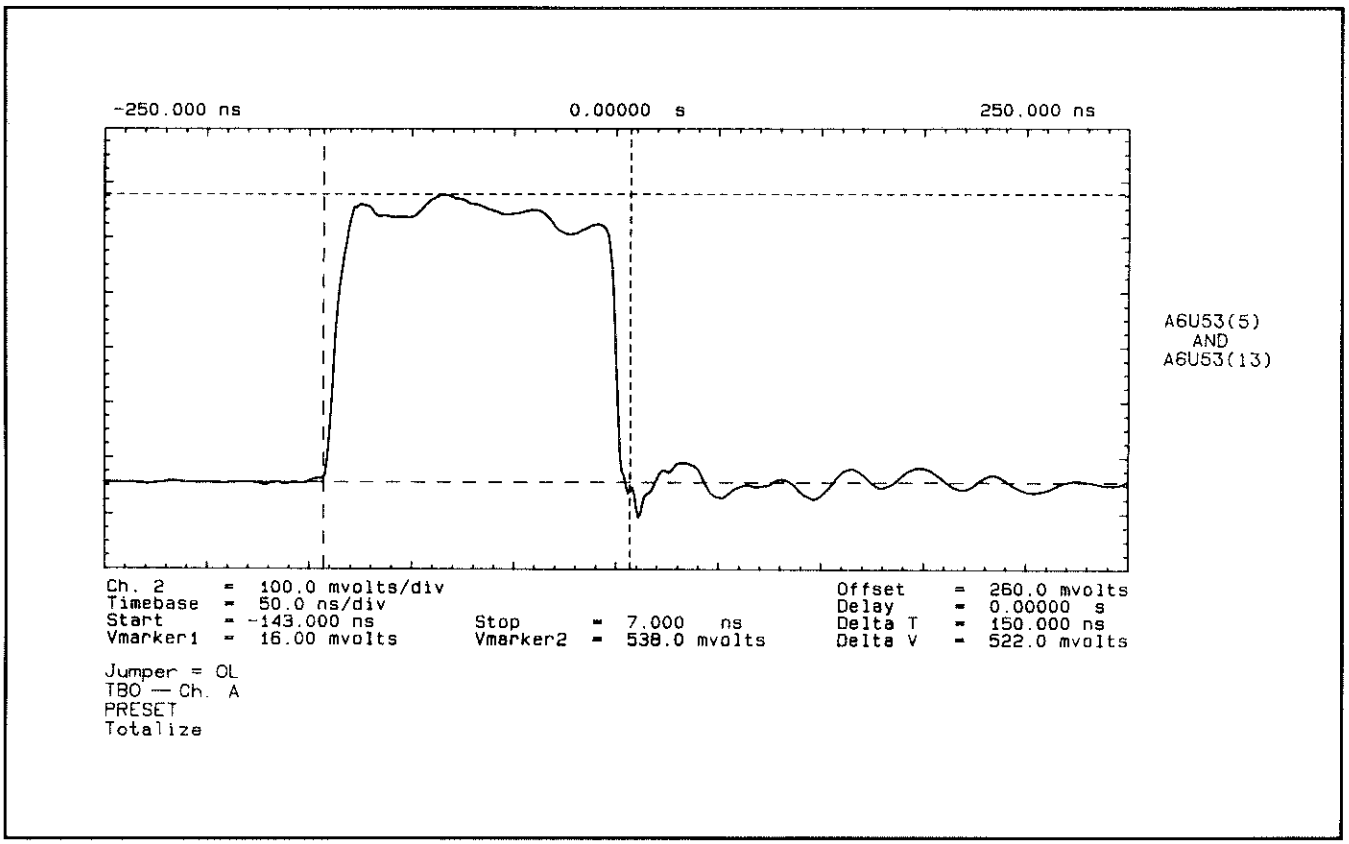


Figure 7F-22. Waveforms at A6U53(5,13) in Totalize Mode

3. Press PRESET. Observe that signals at A6U53(7,15) are as shown is *Figure 7F-23*. Change measurement to Totalize. Observe signals at A6U53(7,15). See *Figure 7F-24*.(Rep Int=10 µSec)

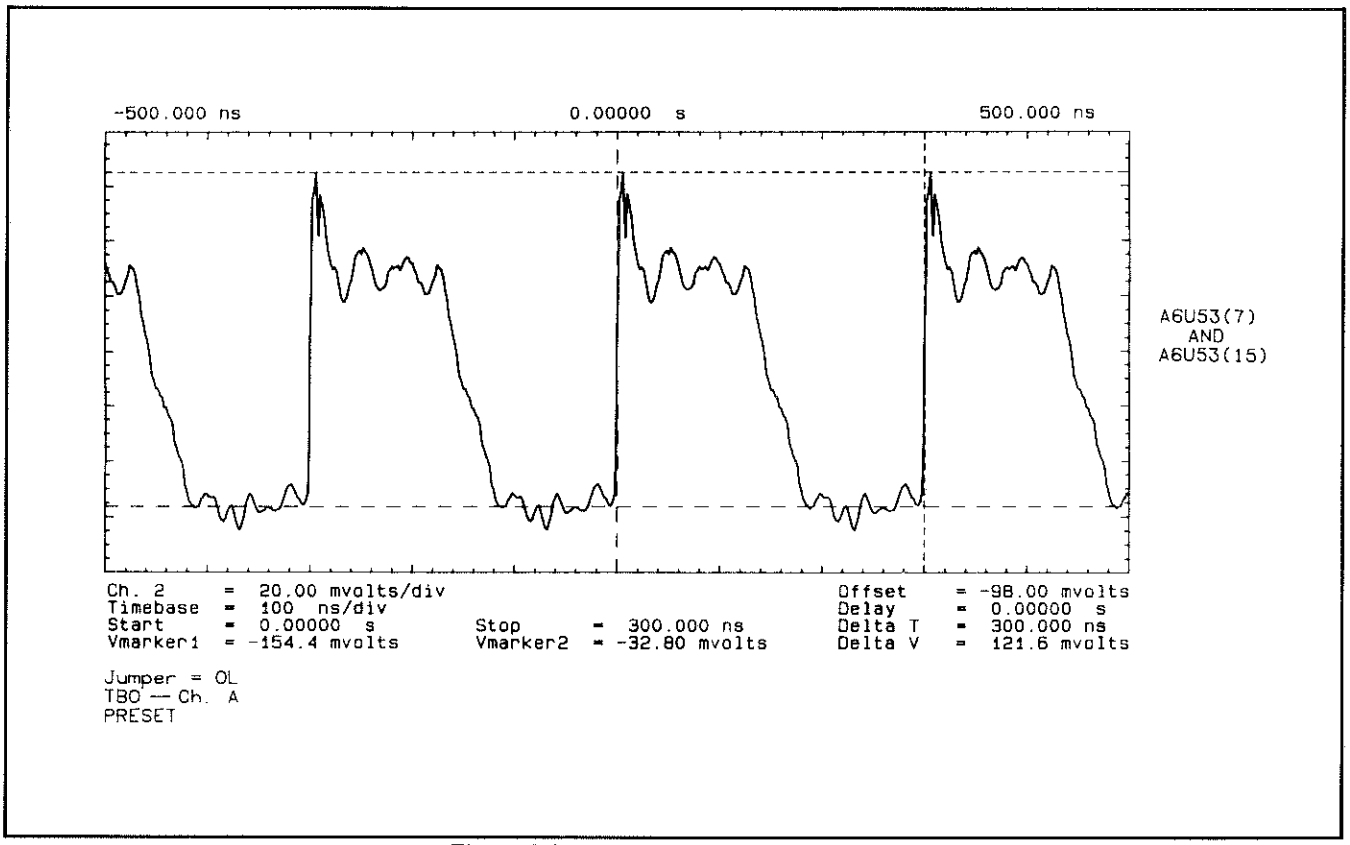


Figure 7F-23. Waveforms at A6U53(7,15)

4. Press PRESET. Observe that signals at A6U53(3,11) are as shown in *Figure 7F-25*. Change measurement to Totalize, check that A6U53(3) goes to ECL Low and A6U53(11) goes ?

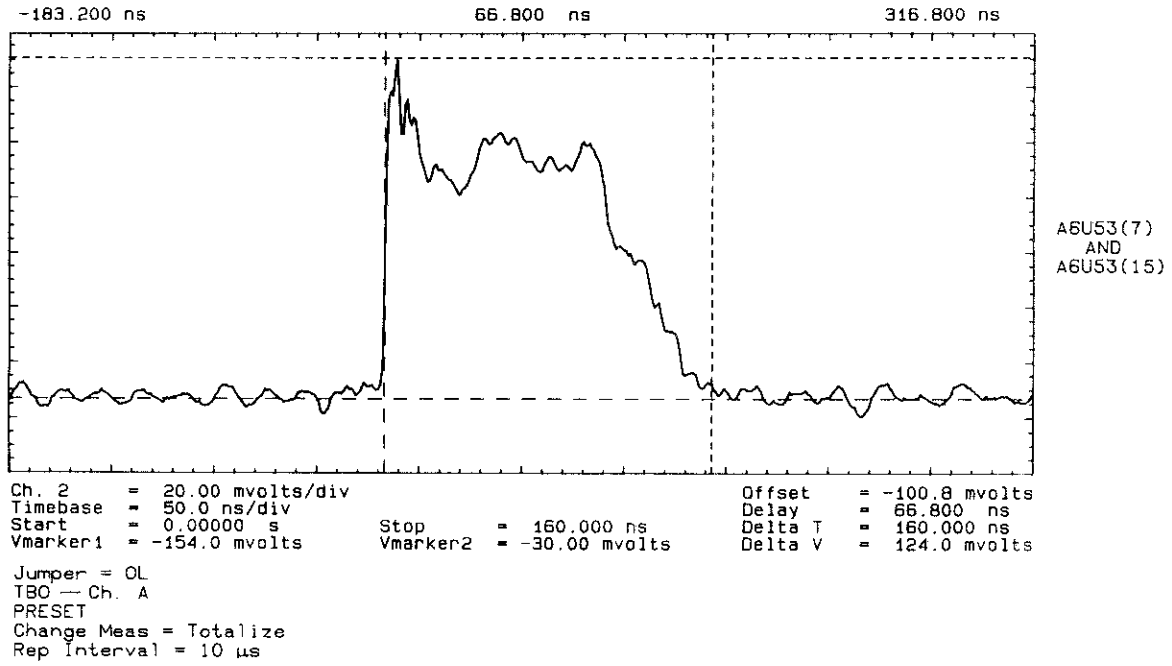


Figure 7F-24. Waveforms at A6U53(7,15) in Totalize Mode

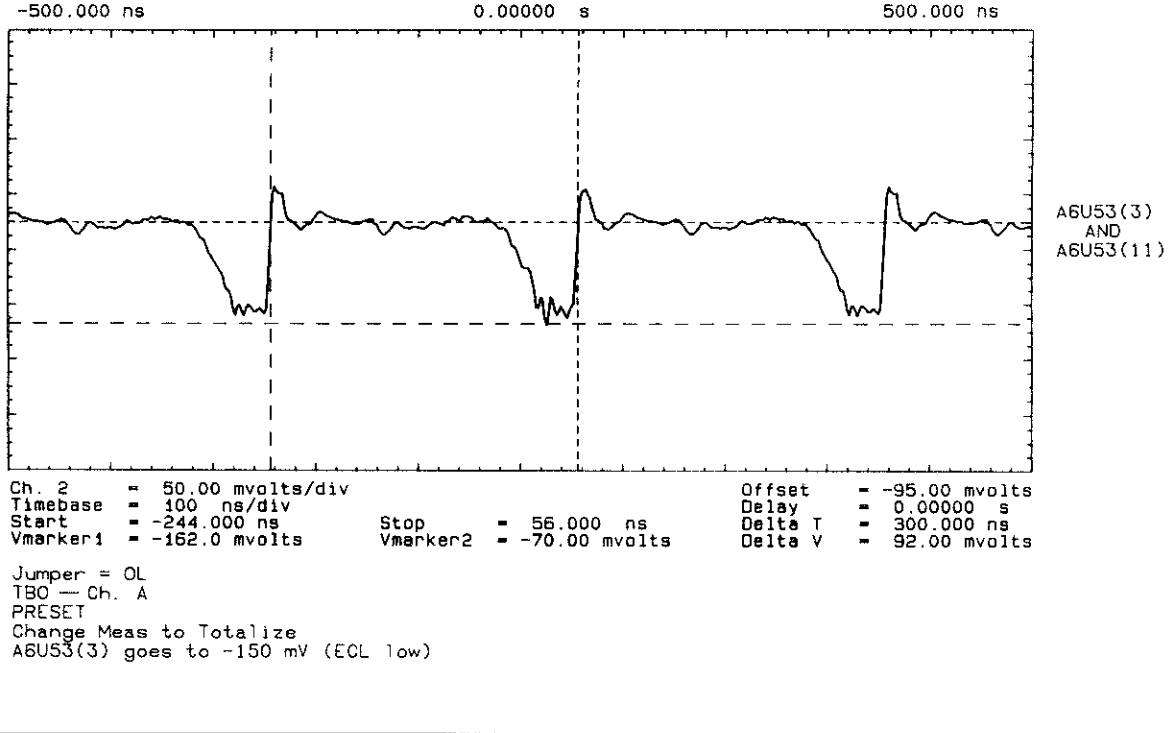


Figure 7F-25. Waveforms at A6U53(3,11)

5. Press PRESET. Observe that signals at A6U53(4,12) are as shown in *Figure 7F-26.* Change measurement to Totalize, check that A6U53(4) goes to ECL Low and A6U53(12) goes ?

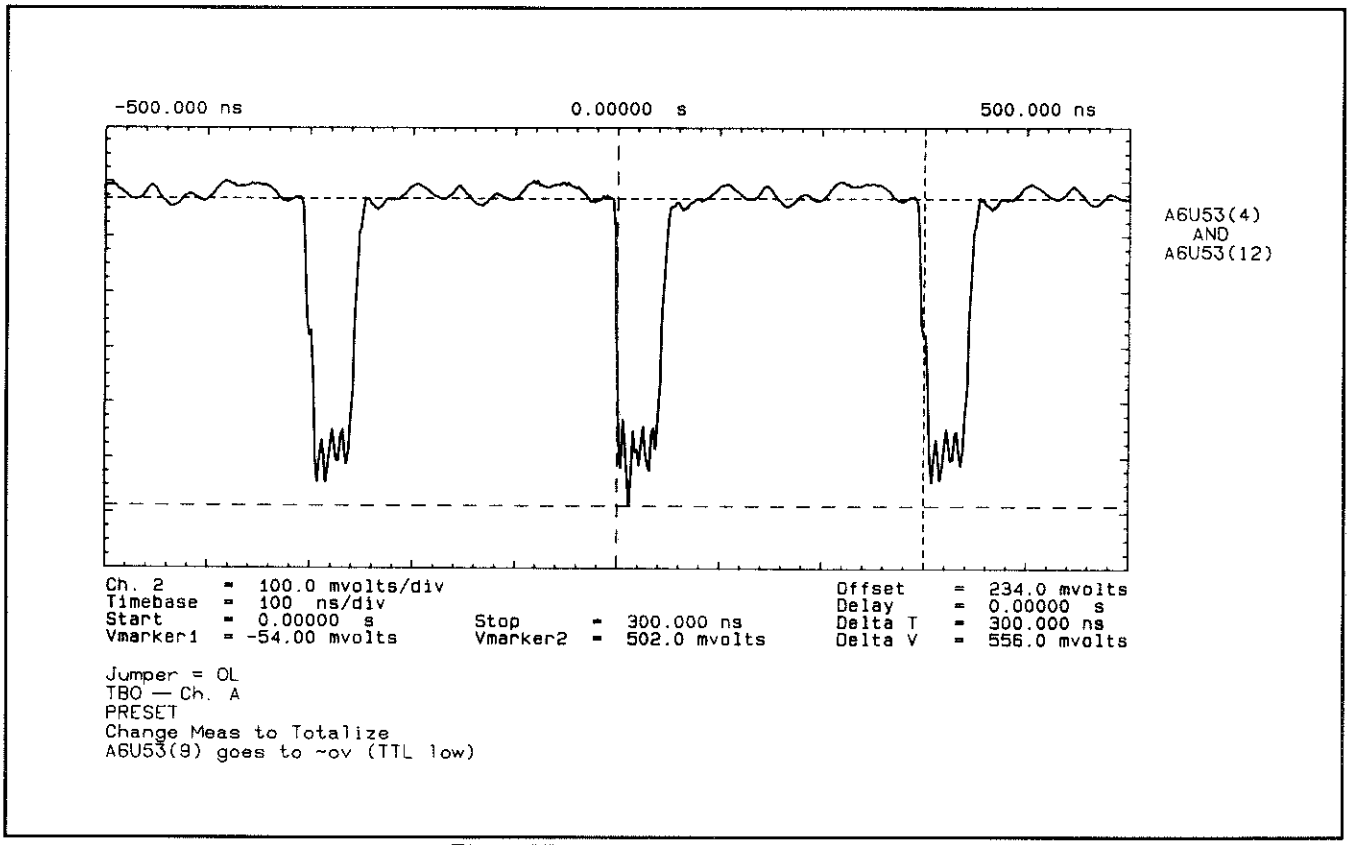


Figure 7F-26. Waveforms at A6U53(4,12)

6. Jumper Position = Open Loop, Timebase Out to Channel A Press PRESET. Observe that signal at A6U39(3) is as shown in *Figure 7F-27.* (Rep Int=300ns) Change measurement to Totalize, check that A6U39(3) goes to TTL Low.

7. Press PRESET. Observe that signal at A6U39(4) is a TTL square wave,(Rep Int=300ns). Change measurement to Totalize. Observe that signals at A6U39(4,6) are as shown in *Figure 7F-28.* (Rep Int=10μs)

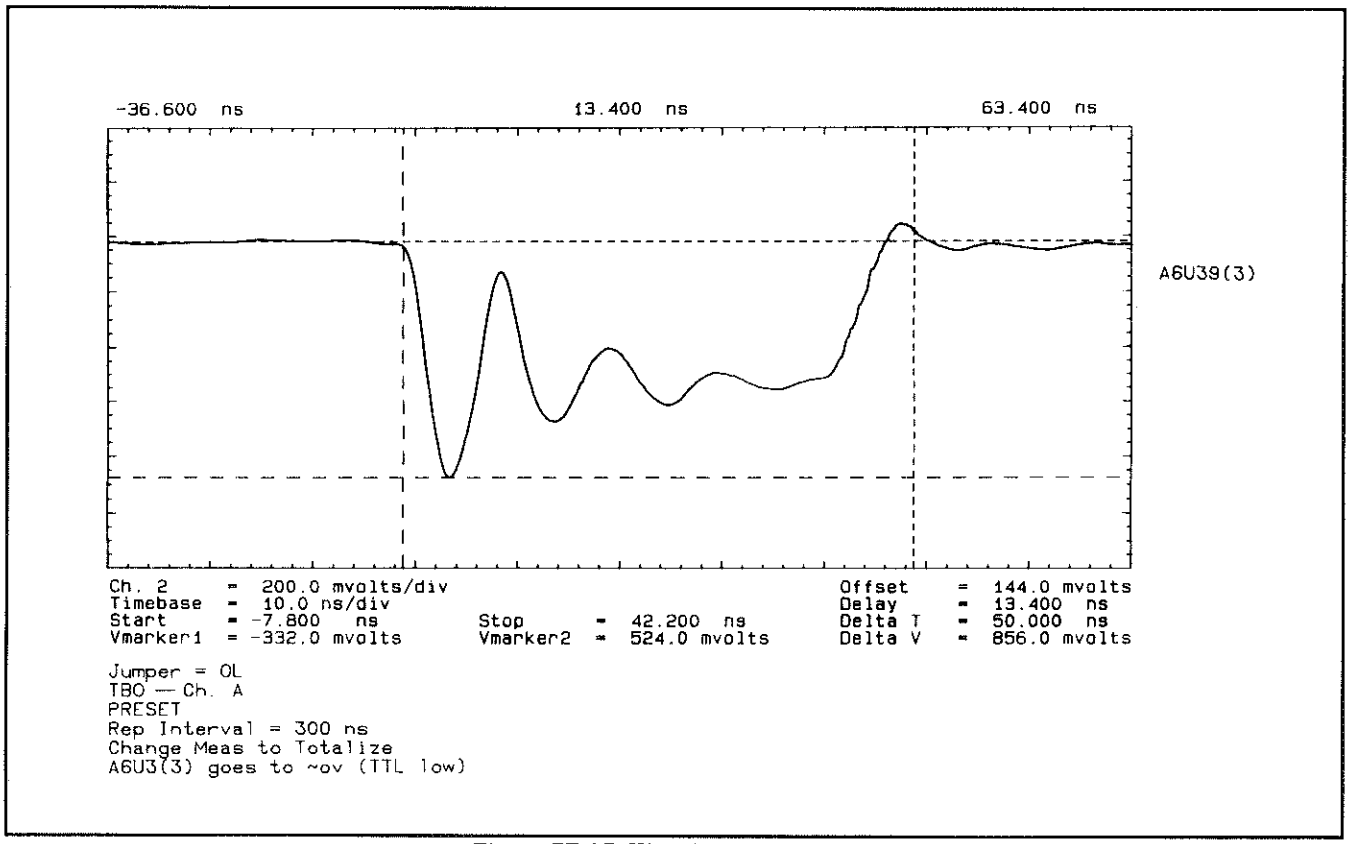


Figure 7F-27. Waveform at A6U39(3)

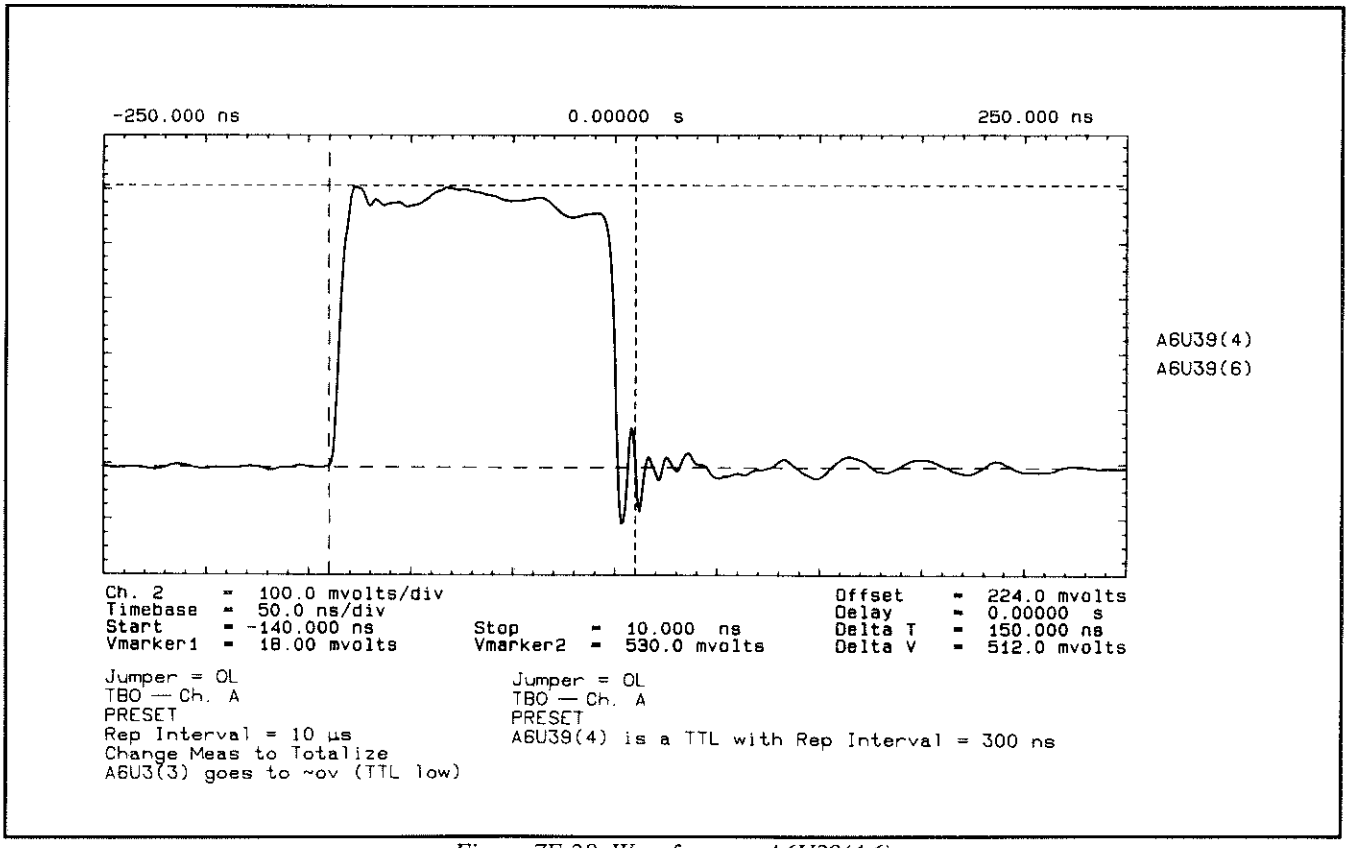


Figure 7F-28. Waveforms at A6U39(4,6)

8. Press PRESET. Observe that signal at A6U39(5) is as shown in *Figure 7F-29*. Change measurement to Totalize, check that A6U39(5) goes to TTL Low.

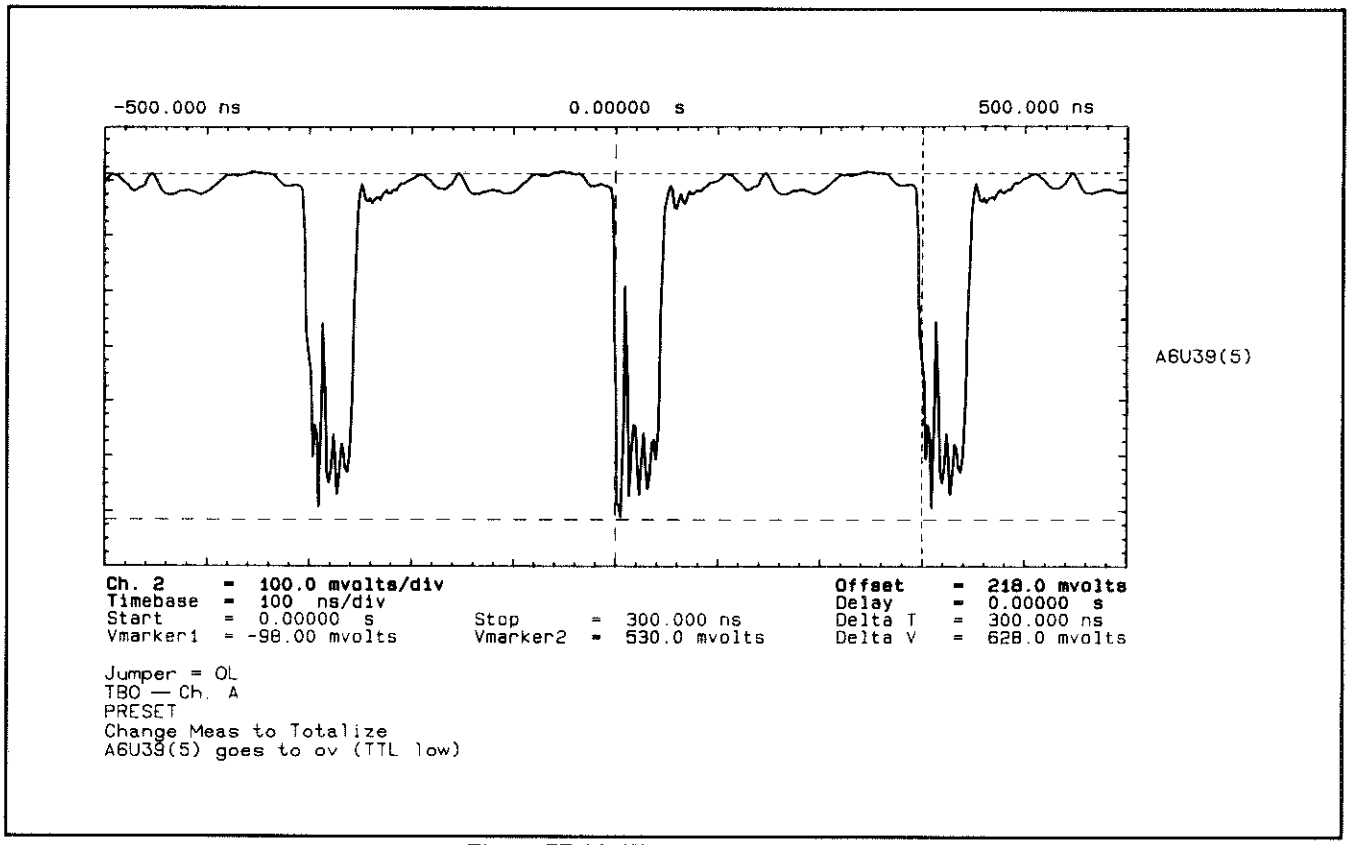
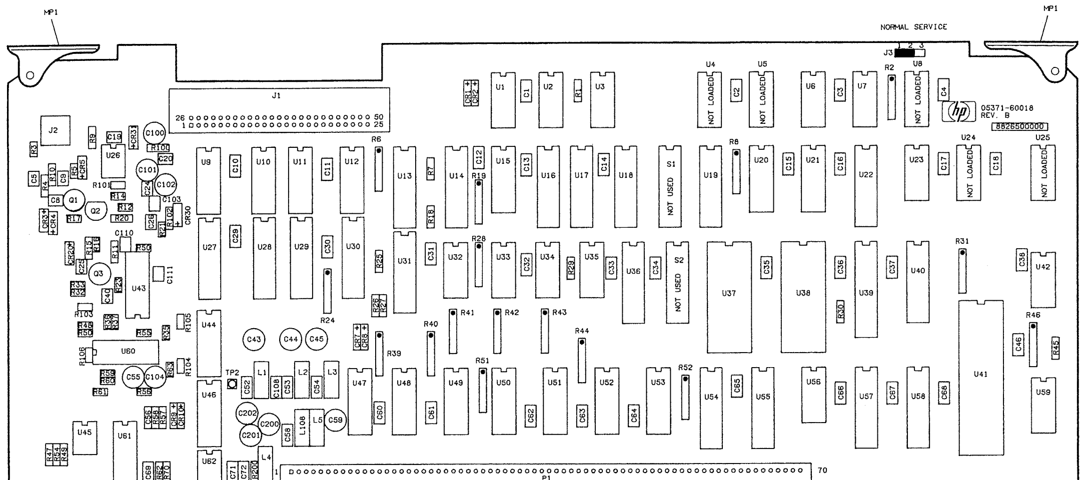


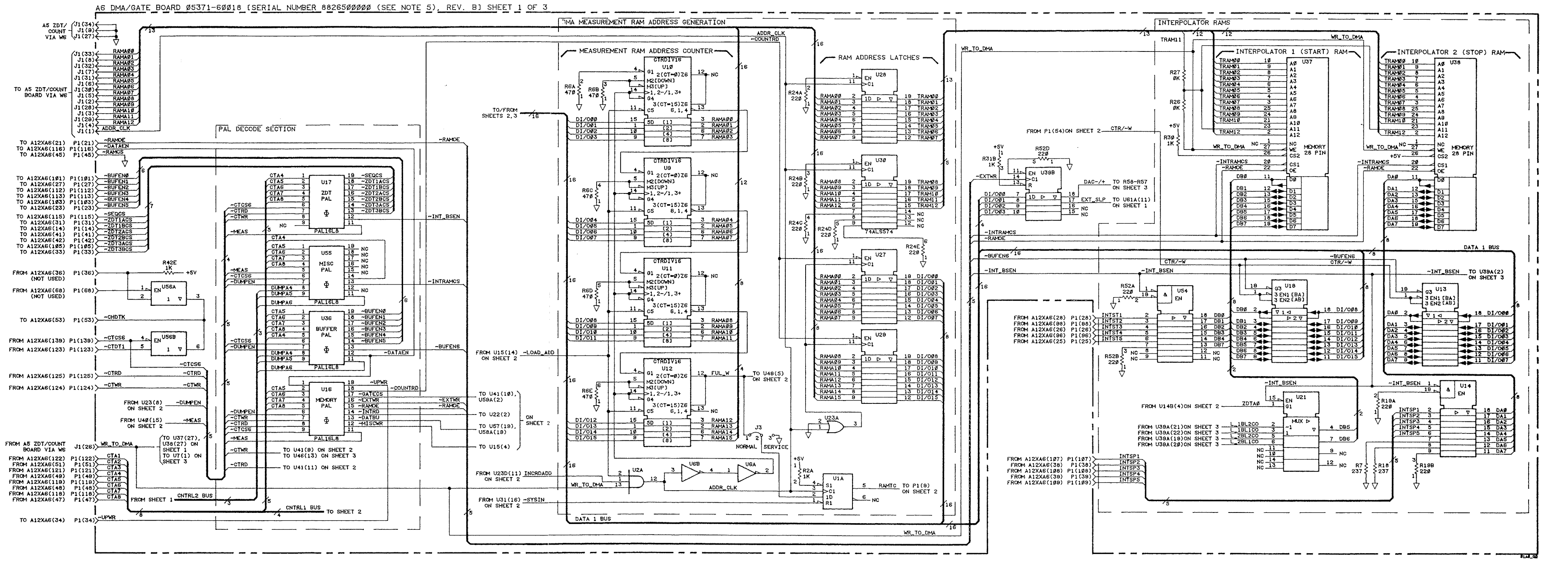
Figure 7F-29. Waveforms at A6U39(5)

9. Press PRESET. Check that A6U39(22) is TTL High. Change measurement to Totalize, check that A6U39(22) goes to TTL Low.

10. Press PRESET. Check that A6U39(21) is TTL High. Change measurement to Totalize, check that A6U39(21) goes to TTL Low.

11. Press PRESET. Check that A6U39(19) is TTL High. Change measurement to Totalize, Check that A6U39(19) is a TTL square wave, Rep Int=10 μs, Pulse Width=75 ns. Press and hold RESTART, check that A6U39(19) goes TTL Low.

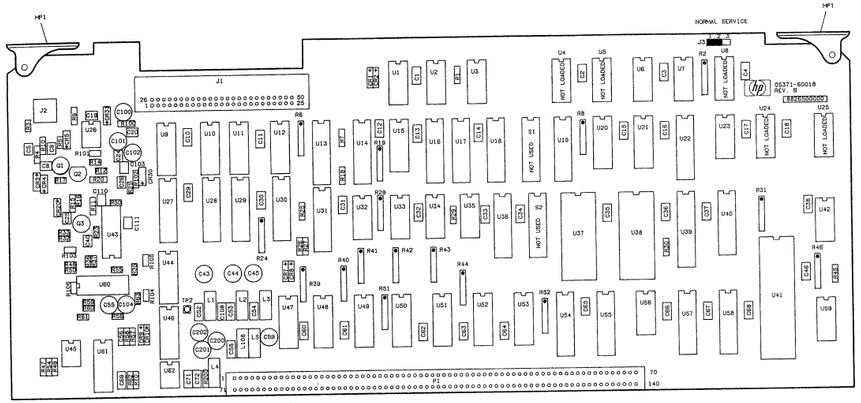




A6 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

Figure 7F-30. A6 DMA/Gate Board Schematic Diagram (Sheet 1 of 3)



A6 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

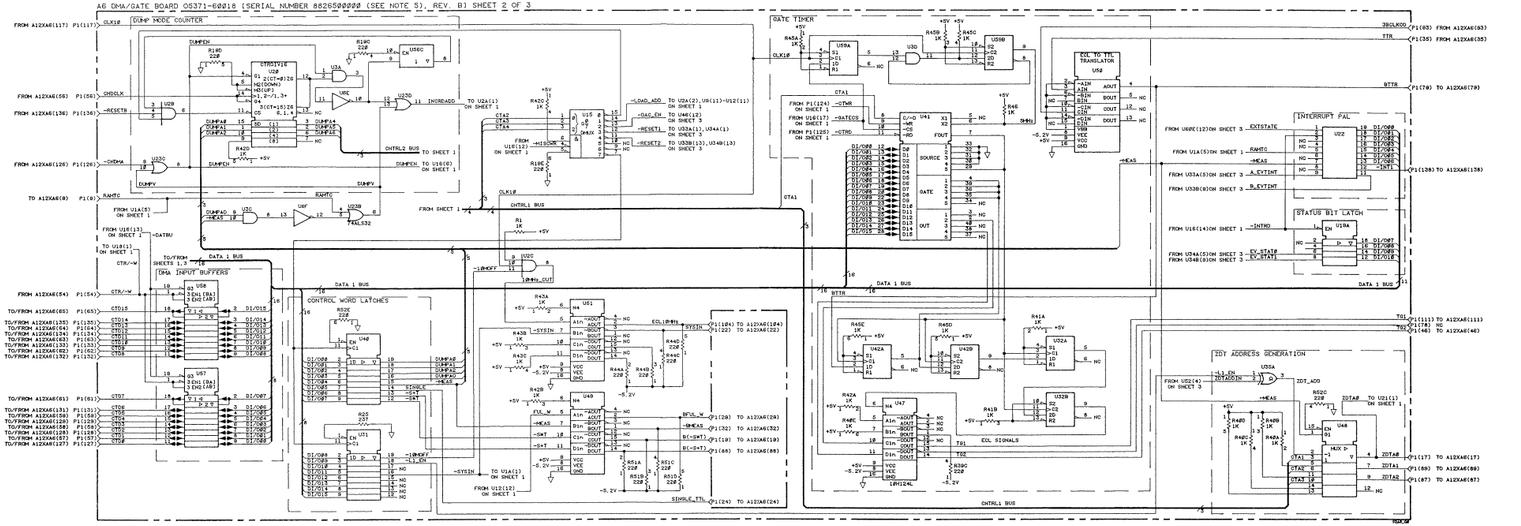
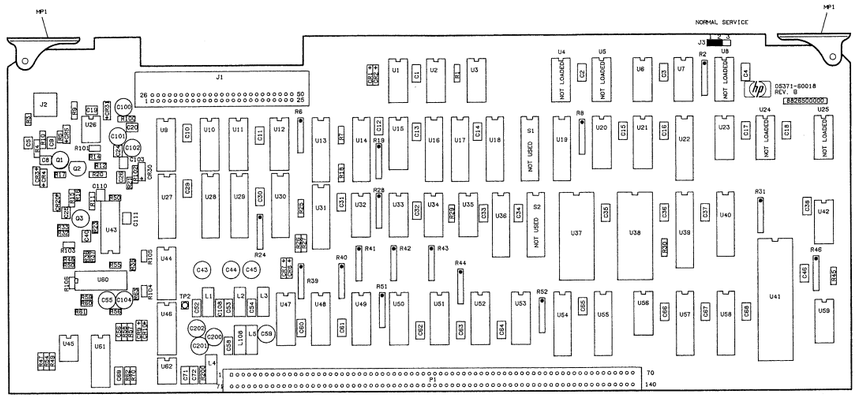


Figure 7F-30. A6 DMA/Gate Board Schematic Diagram (Sheet 2 of 3)



A6 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. RESISTORS R300 AND R301 ARE LOADED ON THE CIRCUIT SIDE OF ALL REVISION A BOARDS.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

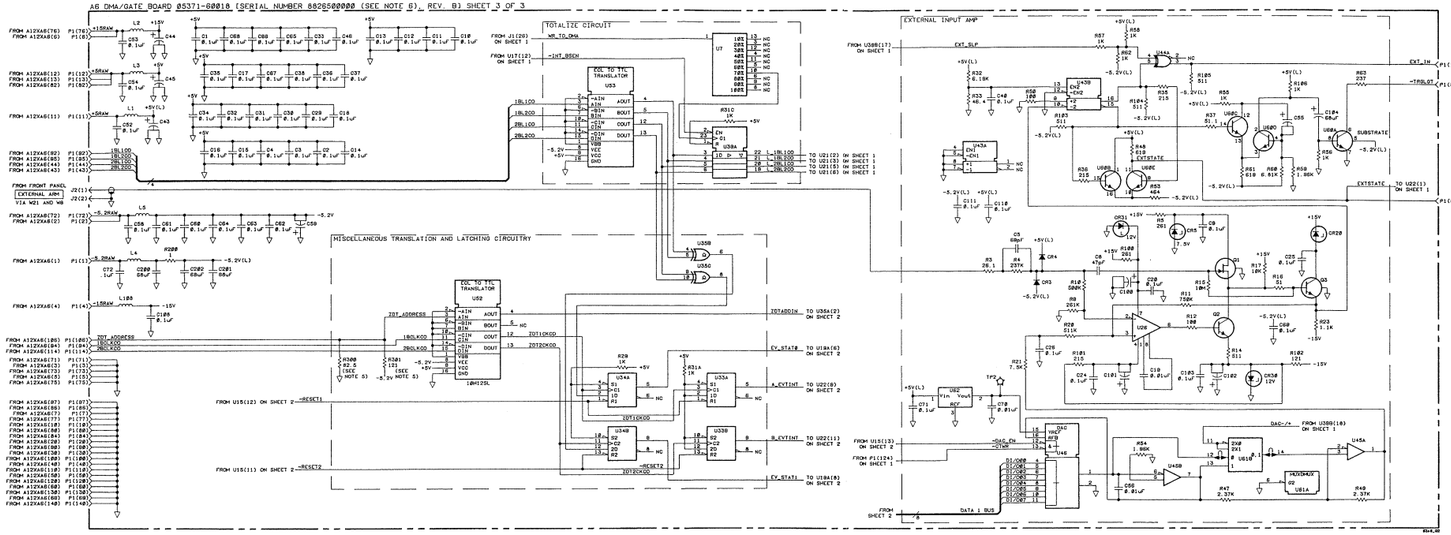


Figure 7F-30. A6 DMA/Gate Board Schematic Diagram (Sheet 3 of 3)

SECTION 7G
A7 PROCESSOR BOARD

7G-1. A7 PROCESSOR BOARD

7G-2. Introduction

The A7 Processor Board and the A8 I/O Controller Board comprise the 5371A control hardware. The A7 assembly performs measurement processing and control while the A8 assembly provides the interface with the user via the front-panel CRT display or an external HP-IB compatible controller. The A7 assembly receives instructions from either the System ROM, the instrument front panel or HP-IB port. It sends the processed measurement to the front-panel CRT display or HP-IB port, and sends the measurement setup control instructions to the counter's measurement hardware. *Figure 7G-1* shows the Processor Board's functional block diagram.

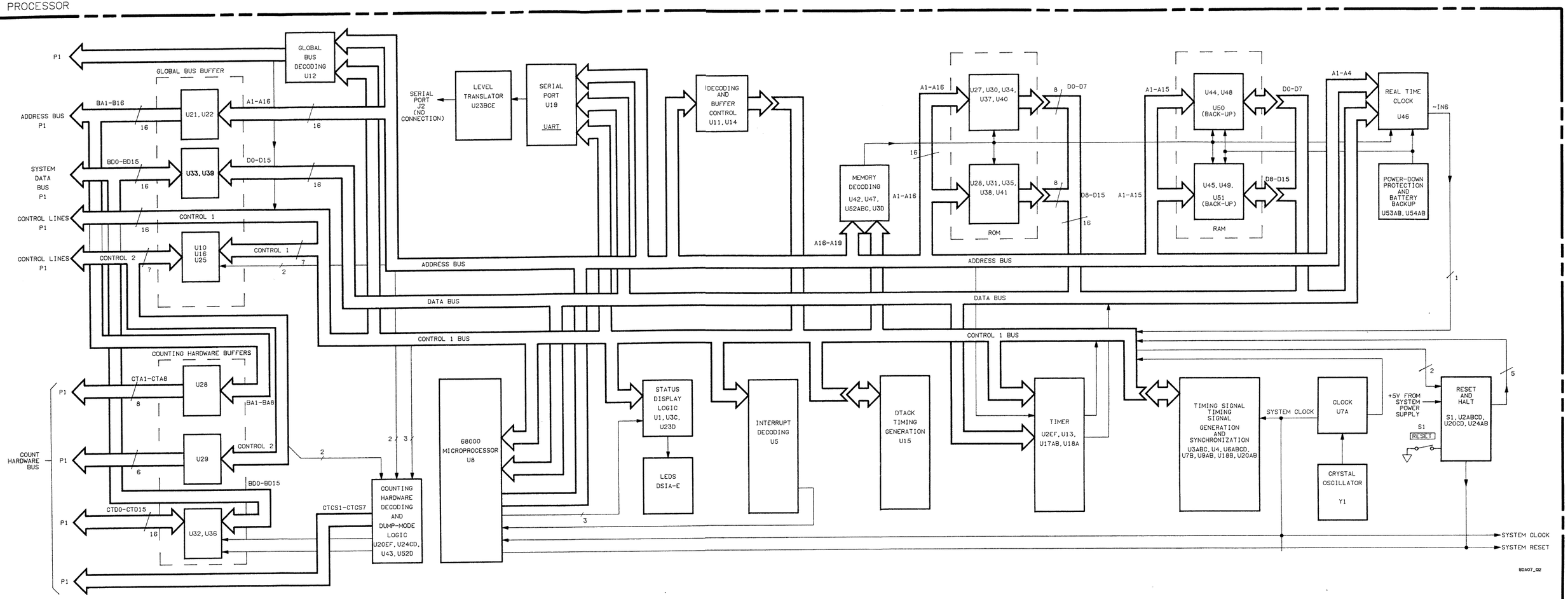


Figure 7G-1. A7 Processor Board Block Diagram

The schematic diagram for the A7 Processor Board is shown in *Figure 7G-8* at the end of this section.

The main functions of the A7 Processor Board include:

- Overall counter operation control by the 68000 μP,
- Decoding logic that determines which device the 68000 μP will communicate with,
- Buffer Circuitry for controlling data flow between circuit elements connected to the CPU kernal's Private Bus, System Bus, and Count Hardware Bus.

The Processor Board's hardware consists of three major sections:

- the 68000 μP-based CPU kernel — comprised of microprocessor and all circuitry that connects directly its Private Bus,
- Decoding Logic — selects which devices the microprocessor is talking to at any given time, and
- the Buffer Circuitry — isolates various parts of the system from each other and provides drive current for the various buses.

7G-3. Central Processor Unit (CPU) Kernel

The central processor's kernel consists of the 10 MHz 68000 Microprocessor (68000 μP), System ROM, System RAM, Real-time Clock Timer, Serial Port, Reset Circuit, Interrupt Handling, Clock Generation, Data Transfer ACKnowledge (~DTACK) Signal Generation, and Address Decoding.

7G-4. 68000 MICROPROCESSOR

A 68000 microprocessor (A7U8) performs all control and measurement functions within the HP 5371A. The processor has the following features:

- a 16-bit data bus
- a 23-bit address bus
- 9.83 MHz UPCLK line
- capable of responding to up to seven levels of interrupts

All 68000 μP signals connect directly to the Private Bus and are buffered to both the System Bus and Count Hardware Bus. The architecture of this uP is beyond the scope of the theory presented here. If interested, additional information is available in the *Motorola Microprocessors Data Manual.*

7G-5. Address Bus

This 23-bit one direction three-state bus provides addressing required for bus operation during all cycles except interrupt cycles. Address lines A1 through A3 identifies interrupt level being serviced during interrupt servicing.

7G-6. Data Bus

This 16-bit bidirectional three-state bus is the general purpose data path for the microprocessor. Data configured in either 16-bit word length or 8-bit byte length can be read over the data bus.

7G-7. Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals:

1. Address Strobe (~AS) — indicates that there is a valid address on the address bus.

2. Read/~Write (R/~W) — defines the data transfer as either a microprocessor read or microprocessor write cycle.

3. Upper and Lower Data Strobes (~UDS and ~LDS) — used in conjunction with R/~W signal to provide control of the data on the data bus. If R/~W is high, the 68000 μP reads from the data as shown in *Table 7G-1*. If R/~W is set low, the microprocessor writes to the data bus as shown in *Table 7G-1*.

Table 7G-1. Data Strobe Control of Data Bus

~UDS	~LDS	R/~W	D8-D15	D0-D7
High	High	–	No Valid Data	No Valid Data
Low	Low	High	Valid Data	Valid Data
High	Low	High	No valid Data	Valid Data
Low	High	High	Valid Data	No Valid Data
Low	Low	Low	Valid Data	Valid Data
High	Low	Low	Valid Data	Valid Data
Low	High	High	Valid Data	Valid Data

4. Data Transfer Acknowledge [~DTACK (~UPDT)] — indicates to the 68000 μP that the data transfer is complete. When ~UPDT is received during a read cycle, data is latched and the bus cycle terminated. When received during a write cycle, the bus cycle is terminated.

7G-8. Bus Arbitration Control

The following three signals for a bus arbitration sequence that determines whether the 68000 μP (A7U8) or DMA Controller IC will control the bus:

1. The Bus Request line (~BR) is generated by the DMA Controller IC, A8U30, when it needs to take control of the bus. When this line is held low, the 68000 μP knows that DMAC wants to take control of the bus.

2. Bus Grant (~BG) informs DMA Controller IC, A8U30, that the 68000 μP will release bus control at the end of the current bus cycle.

3. Bus Grant Acknowledge (~BGACK) informs the 68000 μP that the DMA Controller IC, A8U30, now controls the bus. ~BACK cannot be asserted until (1) ~BG is inactive (high), (2) ~AS is inactive (high) meaning the 68000 μP is not using the bus, (3) ~UPDT, or ~DTACK, is inactive (high) indicating that neither memory nor peripherals are using the bus, and (4) ~BGACK is inactive (high) meaning that no other device is in control of the bus.

7G-9. Interrupt Control

The interrupt control signals indicate the encoded priority level of the 5371A circuit block generating the interrupt. Level seven (~INT7) is the highest priority while level zero indicates that no interrupts are requested.

7G-10. System Control

The system control lines either reset or halt the 68000 μP and to indicate to the microprocessor that bus errors have occurred.

1. Bus Error, ~BERR, notifies the 68000 μP that the bus cycle currently being executed has a problem.

2. The reset line, ~RESET, resets the 68000 μP in response to an external reset signal. Applying an external ~HALT and ~RESET signal simultaneously, which only occurs at powerup or when switch A7S1 is pressed, resets both the 68000 μP and all external devices.

7G-11. Peripheral Control

These control lines allow interfacing between synchronous external devices, such as and the asynchronous 68000 μP.

1. The Enable line, E, provides a 938 KHz, 40% duty cycle enable signal to the CRT Controller A8U12 and the Serial Port UART IC A7U19.

2. Valid Peripheral Address, ~UPVPA, indicates that the device addressed is a MC6800 family device and that data transfer must be synchronized with the enable (E) signal.

3. Valid Memory Address, ~VMA, indicates to MC6800 devices that there is a valid memory address on the address bus and that the 68000 μP is synchronized with the enable line (E).

7G-12. Microprocessor Status

The microprocessor status lines, FC0 through FC2, give an indication of the current microprocessor state and type of bus cycle being executed. These lines drive LEDs A7DS1A through F.

7G-13. SYSTEM ROM

The A7 Processor Board has ten 64K X 8 bit ROMS; A7U27, U28, U30, U31, U34, U35, U37, U38, U40, and U41. The ROMs contain all firmware instructions necessary for the 5371A to function. Each ROM IC has 8-bit data lines. To achieve 16-bit data word, two ROMs are used to form a block of μP memory space. This gives a total ROM memory space of 320K words (or 640K bytes). The ROM space in the 5371A has an address range from 000000 (hexadecimal) to 09FFFF (hexadecimal).

7G-14. SYSTEM RAM

The A7 Processor Board has a total of six static RAM ICs; four 32K × 8-bit (A7U44, U45, U48, and U49) and two 8K × 8-bit ICs (A7U50 and U51). The RAMs are used by the data manager for the execution of software routines, for storage of ASCII and Floating Point data, and for backup storage of setup information, calibration constants, and system information (i.e., HP-IB address). Each RAM has 8-bit data lines. To achieve 16-bit data words, two RAMs are used to form a block of memory space. This gives a total RAM memory space of 72K words (or 144K bytes). The RAM space in the 5371A has an address range from 100000 (hexadecimal) to 12FFFF (hexadecimal).

To facilitate battery backup of selected data, CMOS RAMs are used and battery, A7BT1, is mounted directly on the A7 Processor Board. Data is saved when either the 5371A AC power is lost or the A7 assembly is physically removed from the instrument. In these instances, battery power is applied to RAM ICs A7U50 and U51 via non-volatile power supply, VNV. The battery backup will data for over three years.

OR gate A7U53A maintains the Chip Select 1 pin (pin 20) for backup RAMs A7U50 and U51 high whenever the HP 5371A is in RAM-protect mode. Resistor A7R34 maintains Chip Select voltage to within 0.2 Volts of Vcc during the RAM-protect mode as required.

7G-15. REAL TIME CLOCK

The Real-Time Clock, A7U46, A7U46 tracks years (leap years included), days of the week and time of day. It allows for the CRT display of the current date and time-stamping of selected measurement data. A7U46 also generates a level six interrupt (~INT6) every second which is routed to the 68000 μP. This interrupt allows the update of the CRT display menu every second when the time and date information is being displayed. A7U46 is a CMOS IC and is like the A7U50 and U51 RAMs, are battery protected.

7G-16. TIMER

A7U13 is a 3-channel programmable timer that is used for three time related functions on the A7 assembly. These functions are described below.

1. Counter 0 is a baud rate clock generator for for the Serial Interface Controller (A7U19). This signal is also used to clock the Counter 1, the programmable software interrupt timer. The frequency of this signal is determined by the baud rate required by the serial port. Since a baud rate of 9600 is necessary, the signal must have a frequency equal to 16 × 9600 = 153 600 Hz. This is equal to 68000 μP clock frequency divided by 64. Therefore, Counter 1 divides CLK signal, which is a 9.8304 MHz signal, by 64.

2. Counter 1 is a programmable software interrupt timer. The 5371A can be programmed to place time limits on certain procedures. This counter is programmable between 13 μs to 410 ms in steps of 6.51 μs. Once an interrupt has occurred, it must be cleared by the 68000 μP. Since ~INT6 can also be generated by Real-time Clock A7U46, buffer A7U18A allows the state of Counter 1 to be checked by the 68000 μP.

3. Counter 2 is a bus error watchdog timer. Since the 68000 μP has an asynchronous bus, a timer is required to tell if a bus cycle has taken longer than it should have. Long bus cycles can occur when as the result of a hardware failure or when an undefined location is accessed by the user. The counter will count down from its initial value starting after a rising edge of the Data Strobe (DS) input. DS is asserted at the beginning of every 68000 μP memory access cycle. When the count reaches zero, the counter outputs a pulse. If a rising DS edge is detected before the counter reaches zero, the counter reloads with its initial value and starts counting down again. As long as DS is detected before the counter reaches zero, ~BERR is not asserted. Currently a ~BERR is detected if approximately 60 μS have elapsed between DS signals. Since the ~BERR and ~INT6 signals are wire-ORed, buffers A7U2E and F buffer the outputs of flip-flops A7U17A and B.

7G-17. SERIAL PORT

A7U19 is a Universal Asynchronous Receiver-Transmitter (UART) whose basic function is serial/parallel conversion. It can convert a serial data stream applied at connector J2 into an 8-bit parallel output that can be read by the 68000 μP. Simultaneously, it can convert an 8-bits of parallel data from the 68000 μP into serial data stream output.

The UART has three main sections: the receiver, transmitter, and control. The receiver accepts serial data from J2 clocked at 9600 Hz baud rate and places the data in internal data bus buffers. Since the UART is compatible with the 68000 μP, it uses peripheral control Enable signal (E) to clock the data in the buffers onto the Private Data Bus. In a similar way, 8-bits of parallel data can be clocked from the Private Data Bus into the UART's internal data buffers, converted to a serial data stream, and output to J2 at the 9600 Hz baud rate. The control section accepts control information from the 68000 μP and executes the required instructions. It also generates a level six interrupt, ~INT6, which informs the uP when data has been received or transmitted. The microprocessor responds to the interrupt by reading the UART's status register to verify that the UART had indeed generated the interrupt.

Transistor array A7U23 translates the UART's TXD and RXD outputs from TTL level to RS-232 signal levels of ±12 Volts.

The *Serial Port* is used for in-factory purposes only and is not externally accessible.

7G-18. RESET AND HALT

At instrument power-up, the ~RESET and ~HALT signals must be held low simultaneously to reset the 68000 μP and all external devices. To accomplish this, the A10 Triple Regulator Board must output Power-UP ReSet (~PURST), a 120 mS ± 20% negative pulse generated as the +5-volt supply reaches +4.5 Volts. The ~PURST signal is then buffered by A7U2C and D, generating the ~HALT and ~RESET signals, respectively. These signals are then applied directly to the 68000 μP. ~RESET is buffered twice by A7U20C and D for noise reduction and then distributed throughout the 5371A as ~RESETB.

Single-pole double-throw switch, SW1, which is mounted directly on the A7 board, also allows the user to reset the HP 5371A.

7G-19. SYSTEM INTERRUPT ENCODING

The 68000 μP can respond to seven interrupt levels. These interrupt levels are encoded by priority encoder A7U5. The encoded signals, IPL0-IPL2, are then applied directly to 68000 μP. All interrupts, except the level 6 (~INT6), are generated by hardware that resides off the A7 assembly. ~INT6 is used exclusively by the A7 assembly. *Table 7G-2* lists the interrupt level and the devices within the HP 5371A that generate the each respective interrupt.

Once the interrupt has been received by the 68000 μP, it waits for the current bus cycle to finish and then enters an interrupt-acknowledge cycle. During this cycle, the 68000 μP places the interrupt level on address lines A1-A3 and sets R/~W to read (R). A1-A3 points to the interrupt handling routine in ROM. The ROM location is different for each interrupt level. The microprocessor status lines, FC0-FC2, are set to the interrupt acknowledge function code. The function code is decoded by A7U1 asserting the Interrupt ACKnowledge line (~IACK), and waits for a response via the Valid Peripheral Address line (~UPVPA). This type of interrupt cycle, called an auto-vector cycle, is implemented by ANDing ~IACK and ~VPA through A7U4B, asserting the ~UPVPA signal. Therefore, when an interrupt cycle is initiated, the ~UPVPA is immediately asserted (low) by the ~IACK signal. The 68000 μP asserts both the Address Strobe (~AS) and Lower Data Strobe (~LDS). The ROM places data on data lines D0-D7. The 68000 μP latches the data and releases the ~AS and ~LDS lines.

All interrupts may be disabled for whatever reason by removing jumper A7J2. The removal of A7J2 directly disables priority encoder A7U5.

Table 7G-2. System Interrupts

Generated by	Interrupt Level	Mnemonic	Description
A12 Motherboard	7	~Powerfail(~INT7)	Power Fail Interrupt
A7 Processor	6	~INT6 ~BERR ~INT6 ~INT6	Timer Interrupt Real-time Clock Interrupt Serial Port Interrupt
A8 I/O Controller	5	~INT5	Keyboard Controller Interrupt
A8 I/O Controller	4	~INT4	HP-IB Controller Interrupt DMA Complete Interrupt
A1 Timebase Control	3	~INT3	Overvoltage Interrupt Input Pod Removed Interrupt
A1 Timebase Control	2	~INT2	Oscillator Out-of-Lock Interrupt Oscillator Source Change Interrupt
A6 DMA/Gate	1	~INT1	Measurement Complete Interrupt Zero Dead Time (ZDT) Overflow Interrupt

7G-20. CLOCK GENERATION

Socket-mounted crystal, A7Y1, generates 19.6608 MHz the system clock used by the 68000 μP. This clock frequency was selected for the following three reasons. First, the 19.6608 MHz contains no harmonics near the 500 MHz reference frequency, which is used by the 5371A count hardware. Harmonic generation could interfere with the phase-locked loop circuit located on the A14 Timebase Multiplier Board. Second, the 19.6608 MHz is used to generate the BAUD RATE (9600 Hz) required by the Serial Port. And thirdly, the 19.6608 MHz is used to generate the 60 Hz CRT frequencies. Divide-by-two flip-flop A7U7A provides the 68000 μP with the required 9.8304 MHz clock input, UPCLK. OR gate A7U3B, buffers the clock signal and distributes the clock to the rest of the Processor Board's circuitry.

7G-21. DTACK TIMING GENERATION

This circuit generates the 68000 μP DTACK responses for data transfers that occur over the Private and System Buses, ~KRDTK and ~DTACK respectively. The 68000 μP operates asynchronously during data transfers. When it wants to transfer data over the bus, the uP activates the data strobe lines (~UDS and ~LDS) to indicate a data transfer is occurring. Data is then read from or written to the peripheral or memory depending on the state of the Read/~Write (R/~W) line. Once the data transfer is complete, the data transfer acknowledge signal (~DTACK) is returned to the 68000 μP indicating the bus cycle is complete. The μP may now proceed with the next operation.

Serial shift register, A7U15, which is clocked from the 9.8304 MHz system clock (CLK), generates the DTACK signals. The data strobe signal, DS, is applied to the serial input of the shift register. This circuit generates four separate GDTn signals (Generate DTACK) GDT1, GDT2, GDT3 and GDT5. Each signal lags the previous one by 100 ns. The first signal, GDT1, is generated approximately 110 ns after the beginning of the bus cycle. Other 5371 assemblies use the GDT signals to generate their own ~DTACK responses for the 68000 μP. The bus cycle time (or access time of the selected IC) depends on which GDT line is used to generate the ~DTACK signal.

7G-22. MEMORY DECODING

The *Memory Decoding* block uses upper address lines A16-A19 to enable either System ROM or System RAM ICs and select which 16-bit memory word has access to the Private Data Bus. All control signals are provided directly from the 68000 μP or Address Decode PAL IC, A7U14. OR gates A7U52A and U52B determine whether the System ROM or System RAM devices have access to the data bus. Decoder A7U42 selects which System ROM pair – A7U27 and U28, U30 and U31, U34 and U35, U37 and U38, or U40 and U41 – will output a 16-bit word to the data bus. Decoder A7U47 selects which pair of System RAM ICs – A7U44 and U45, U48 and U49, or non-volatile RAMS U50 and U51 – can be written to or read from. OR gates A7U52C and U3D determine whether the upper byte (D8-D15) or lower byte (D0-D7) has access to the data bus. The Chip Select signals to the non-volatile RAMs, A7U50 and U51, are routed through the *Power-Down Protection and Battery Back-up* before being sent to non-volatile RAM ICs A7U50 and U51. (See *Power-Down Protection and Battery Back-Up* for theory of operation.)

7G-23. DECODING AND BUFFER CONTROL

This circuit consists of two uniquely programmed Programmable Array Logic devices (PALs), A7U11 and A7U14, that respectively serve as buffer and address decoders for A7 Processor Board circuitry. *Table 7G-3* provides information on PAL input/output signals.

Table 7G-3. Buffer Control and Address Decode PAL Pinouts

PAL Name	Power Pin	Gnd Pin	Input Pins	Output Pins	Signal Names
Buffer Control (A7U11)			1		Address Strobe
			2		Valid Memory Address
			3		Address Line 23
			4		Address Line 22
			5		Address Line 21
			6		Address Line 20
			7		Address Line 19
			8		Memory – Direct Memory Access
			9		Bus Grant Acknowledge
		10			
			11		Read/Write
				12	Kernel Valid Peripheral Address
				13	RS-232 Chip Select
				14	Kernel Enable
				15	Data Bus Direction
				16	Latch or Pass Through
				17	Address Buffer Direction
				18	Address Buffer Enable
				19	Bus Enable
	20				
Address Decode (A7U14)			1		Address Line 16
			2		Address Line 17
			3		Address Line 18
			4		Address Line 19
			5		Address Line 20
			6		Address Strobe
			7		Address Buffer Direction
			8		Generate Data Transfer 1
			9		Data Strobe
		10			
			11		Generate Data Transfer 5
				12	Timer State Enable A7U18(1)
				13	Kernel Enable
				14	Real-Time Clock Chip Select
				15	RAM Chip Select
				16	ROM Chip Select
				17	Timer Chip Select
				18	Timer Interrupt Clear
				19	Kernel Data Transfer Acknowledge
	20				

7G-24. GLOBAL BUS DECODING

The *Global Bus Decoding* IC, A7U12, decodes address lines A19, A20, and A21 generating Board Select ~BS3 and *Count Hardware Buffer* Chip Select ~CHCS signals. ~BS3 enables decoder A8U36 (located on the A8 I/O Controller Board) which decodes address lines A15, A16, and A17, generating A8 I/O Controller Board block selection signals ~SEL0 through ~SEL7. ~CHCS, the Count Hardware Chip Select line, directly enables the Count Hardware control line buffer A7U29 and address buffer A7U26. ~CHCS is also decoded by the logic circuits of *Count Hardware Decoding and Dump Mode Logic* block and used by Count Hardware Data buffers A7U32 and U36.

7G-25. COUNT HARDWARE DECODING AND DUMP MODE LOGIC

7G-26. Timing Signal Generation and Synchronization

This circuit performs three functions. It synchronizes all data transfer acknowledge signals, which are generated after transfer of data over the Count Hardware Data Bus (~CHDTK), the System Data Bus (~DTACK), and the 68000 μP's Private Data Bus (~KRDTK), with the 9.83 MHz microprocessor clock (UPCLK). In addition, this circuit ensures proper timing of the 68000 μP memory/peripheral read and write cycles. And finally, this circuit implements the Auto-vectored interrupt function (see *System Interrupt Decoding* for more details).

7G-27. Count Hardware Bus Buffers

The *Count Hardware Buffers* isolate the Count Hardware Bus from the System Bus. A7U29 buffers the control lines, A7U26 buffers the address lines, while A7U32 and U36 buffer the sixteen data lines. This arrangement isolates the noise generated on the System Bus from the Count Hardware Bus. All four buffers are controlled by the ~CHCS signal, which is generated by A7U12 of the *Global Bus Decoding* circuit. The buffers remain off until the 68000 μP wants to access the Count Hardware Bus.

The Count Hardware Data Bus buffers, A7U32 and U36, are also turned on during DMA transfer of unprocessed measurement data from the A5 ZDT/Count and A6 DMA/Gate Boards to the *HP-IB Control Circuit* located on the A8 I/O Controller Board.

7G-28. Global Bus Buffers

The main function of the *Global Bus Buffers* is to isolate the 68000 μP's Private Bus from the System Bus. The two buses may be isolated when testing of the kernel is to take place. In addition, the buffers provide the drive current required to interface with the A8 I/O Controller Board via the System Bus. The System Bus allows communication with all devices on the A8 assembly. Transceivers A7U33 and U39 buffer the data bus (D0 through D15), transceiver A7U22 and U21 buffer the address bus (A0 through A16), and transceiver A7U25 buffers seven control lines. A7U21, U22, and U25 remain on unless the *DMA Controller Circuit*, which is located on the A8 I/O Controller Board, requests the bus. When another processor requests the bus, the address and control buffers are turned off by asserting the ~BGACK signal. However, if a DMA cycle is performed on data to or from the System RAM, signal ~MEDMA is asserted turning the three buffers on. This allows the *DMA Controller* to send address and control information to the A7 Processor Board. Transceiver enabling and direction of data flow is programmed by PAL IC A7U11.

7G-29. Status Display Logic

The 68000 μP outputs a 3-bit function code on lines FC0, FC1, and FC2 (pins 28, 27, and 26 respectively) which indicates what activity is currently in progress. These lines are valid when the microprocessor's address strobe ~AS is active (low). A7U1 decodes FC0-FC2 and drive LEDs A7DS1E-F. These LEDs give a visual indication as to the status of the microprocessor. The "interrupt acknowledge" status (A7U1 pin 7) is decoded and and used to drive LED A7DS1A. It also is ORed with address strobe line ~AS by gate A7U3C. The output of A7U3C, ~IACK, is distributed throughout the HP 5371A.

7G-30. Power-Down Protection and Battery Back-Up

The Real Time Clock (U46) and non-volatile RAMs (U50 and U51) receive backup power from a non-rechargable battery (lithium) BT1 mounted directly on the A7 Processor Board. By mounting the battery directly on the A7 assembly, the assembly can be removed from the HP 5371A chassis without loss of data. The chassis-mounted power transformer T1 provides power to the A7 assembly and the oven oscillator whenever the HP 5371A is connected to line voltage regardless of whether the front panel power switch is set to ON or STBY. This "hot" line is regulated on the A7 assembly by a 5.6 Volt zener diode. The regulated non-volatile power supply (VNV) is protected from the "hot" line being shorted to ground by diode CR3. Diode CR4 allows current to flow into the non-volatile power supply (VNV) when the HP 5371A power switch is set to ON position. Diode CR5 and resistor R33 protect the battery (BT1) from being charged whenever the supply voltages are on (front panel power switch set to ON position), non-volatile power supply (VNV) is equal to +5 Volts, or from excessive current should VNV short to ground. Capacitor C43 decouples the non-volatile power supply (VNV).

The Battery Backup and Power-Fail protect circuit consists of CMOS flip-flop U54A, OR gates U53A,B, and C), and Power-fail interrupt (~INT7). This circuit protects CMOS RAMs U50 and U51 and Real Time Clock (U46) during an HP 5371A system power failure, ensuring that the data stored in RAM remains valid until power is reconnected. To ensure that the RAM data is valid after the power returns, the 68000 μP does a check sum of the memory contents prior to the instrument's losing power. The Power-fail interrupt (~INT7) informs the microprocessor of the impending power loss. The processor suspends its current activity, opens the front-end relays (located on the A2 Input Amplifier Assembly), and performs a check sum on the U50 and U51 CMOS RAMs. To accomplish this task, the microproces-

sor first writes to a RAM memory location. This clocks CMOS flip-flop U54A which sets its output to zero. Since the ~RESET line connects to the CLEAR input of U54A, the flip-flop remains in the "cleared" state through system power-up. U54A's inverted output is routed to one input of each of the three CMOS OR gates (U53A,B, and C). The other inputs to the OR gate are the chip-select signals for RAMs (U50 and U51) and the Real Time Clock (U46). The outputs of the OR gates are routed to the respective chip-select inputs of the RAMs and Real Time Clock.

The Real Time Clock U46 and the back-up RAMs U50 and U51 go into their low-power modes at approximately 4 Volts and 4.5 Volts respectively. The RAM chip-select pins (Pin 20) voltage must be held to within 0.2 Volts of Vcc. R34 ensures that the chip select voltage level is maintained by connecting the pins to the non-volatile power supply (VNV).

7G-31. A7 PROCESSOR TROUBLESHOOTING

Symptoms:

The six LEDs near the front panel are helpful in determining the condition of the HP 5371.

Under normal operation, after the HP5371 has been turned on, the 4th and 5th LEDs (SUP DATA and SUP PROG) light up while the 2nd and the 3rd LEDs (USER DATA and USER PROG) flash. Moreover, when the red RESET button next to the LED's are pressed, the 1st and 6th LEDs (HALT and RESET) light up simultaneously. If any of the six LEDs do not operate as indicated above, the A7 board should be checked.

Diagnosis:

Clock Signal:

A. Measure the clock signal at A7U7(3) for a 50 ns period (approximate sine wave). See *Figure 7G-2.*

If the clock signal is incorrect, replace A7Y1, the crystal oscillator.

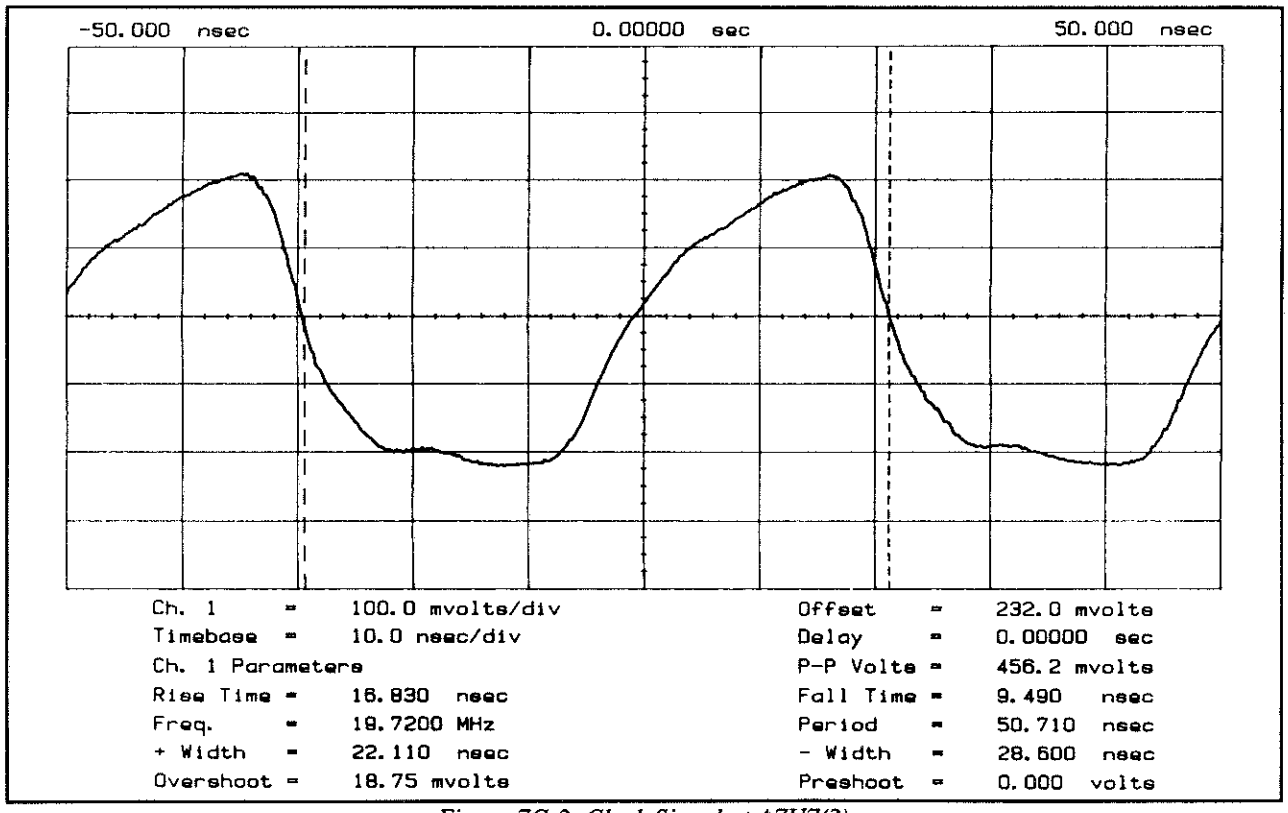


Figure 7G-2. Clock Signal at A7U7(3)

B. Check for a 100 ns period at A7U7(5) and A7U3(6). If any of the signal is incorrect, the problem lies in the two IC's.

Reset and Halt Circuits:

A. Verify that both A7U2(6) and A7U2(8) are high. If not, replace A7U24.

68000 Processor:

A. Set the microprocessor into a free-running state by positioning the J5 and J6 jumpers in the LEFT position, removing the J2 and J4 jumpers, and moving J3 jumper to clamp on the 2nd and 3rd pins rather than on the 1st and 2nd pins.

B. Verify the following signals at A7U8, the microprocessor:

Pins	Signal
15	100 ns clock
22	High
17	High
18	High
21	High
25	High
24	High
23	High
10	400 ns period (See *Figure 7G-3*).
13	High
12	High

C. Verify the following signals at Microprocessor A7U8:

Pins	Signal
20	1 μs period (See *Figure 7G-4*)
19	High
6	400 ns period (See *Figure 7G-5*)
9	High
7	400 ns period
8	400 ns period
11	High
28	Low
27	High
26	High

D. Check the address lines of A7U8 at pin 29 through 34. (See *Figure 7G-6*).

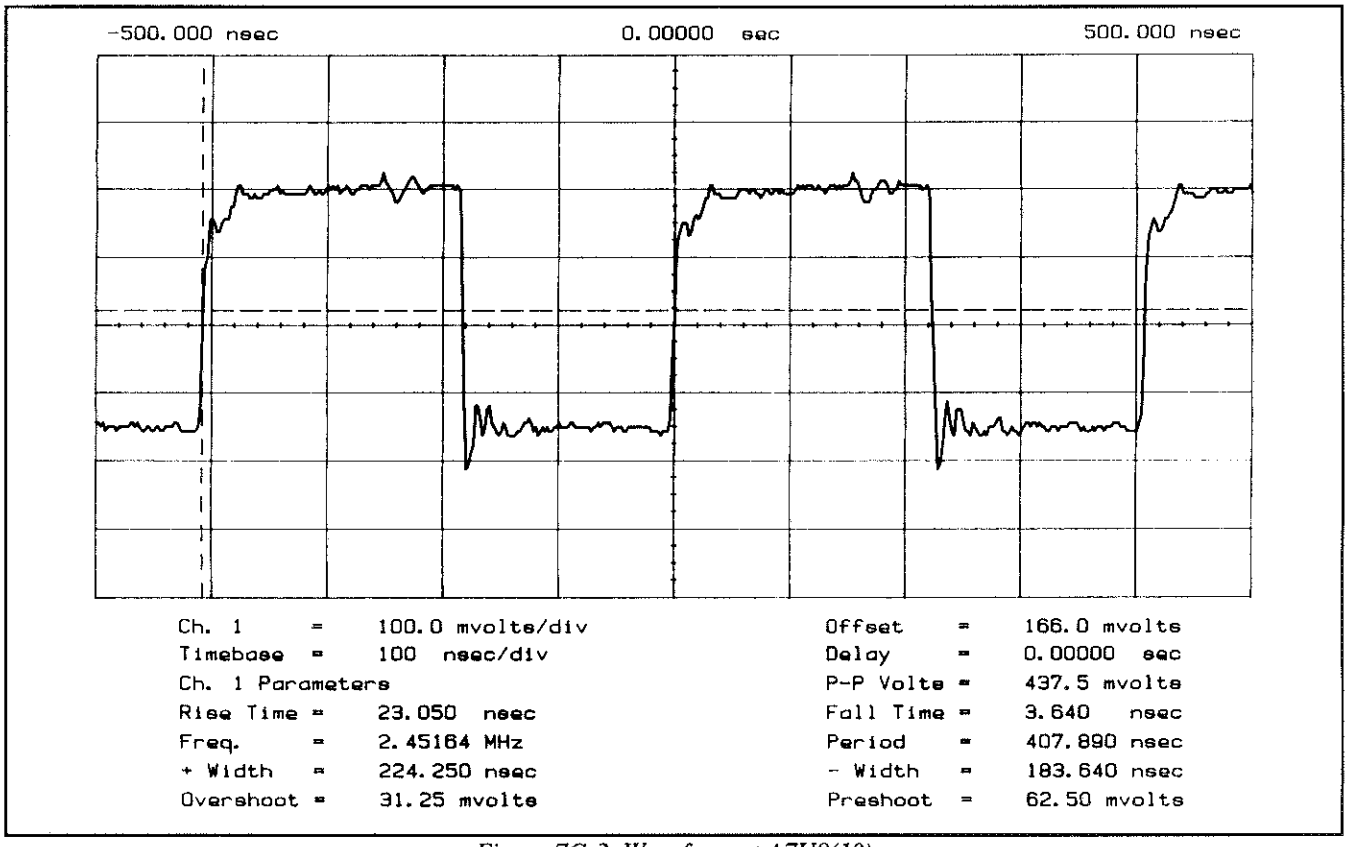


Figure 7G-3. Waveform at A7U8(10)

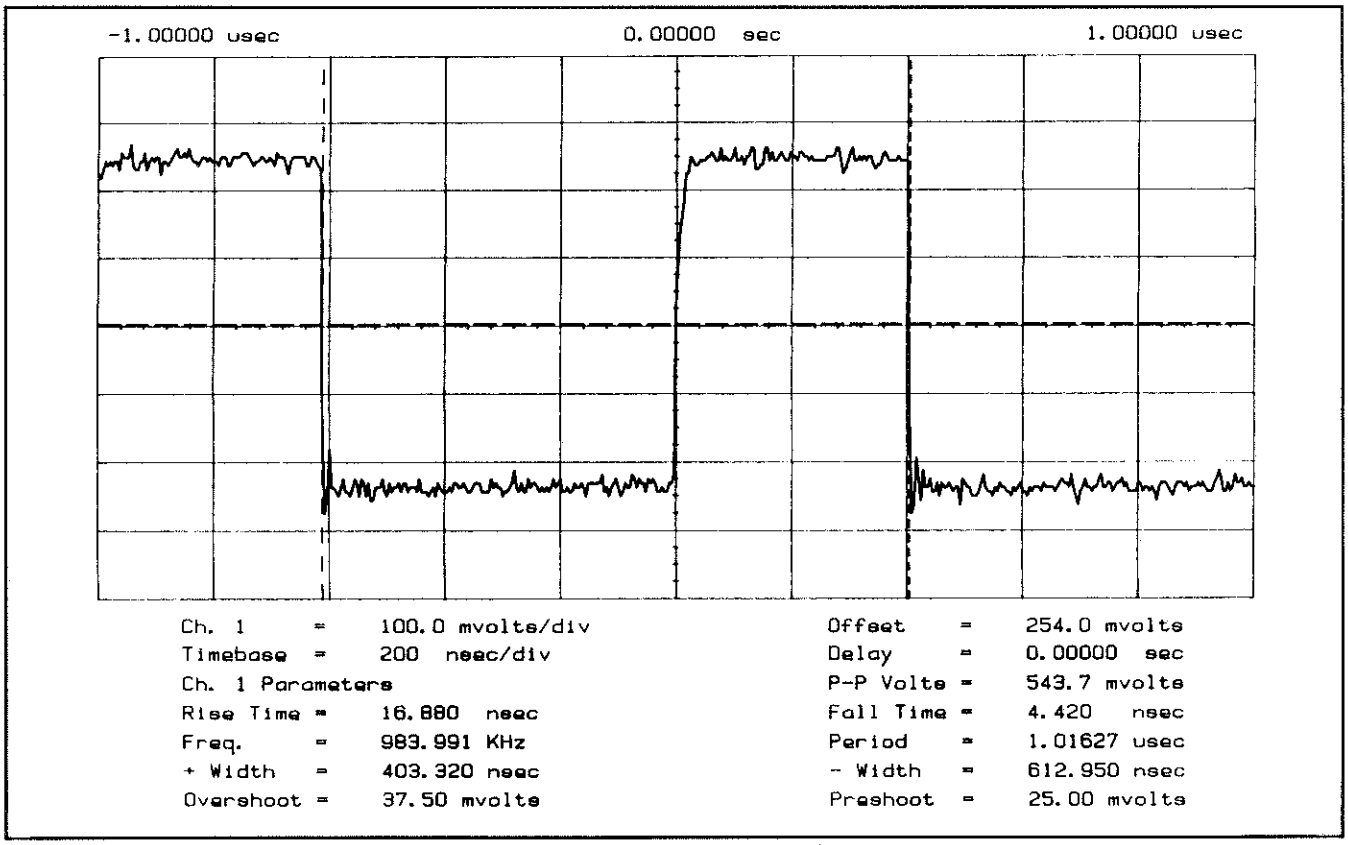


Figure 7G-4. Waveforms at A7U8(20)

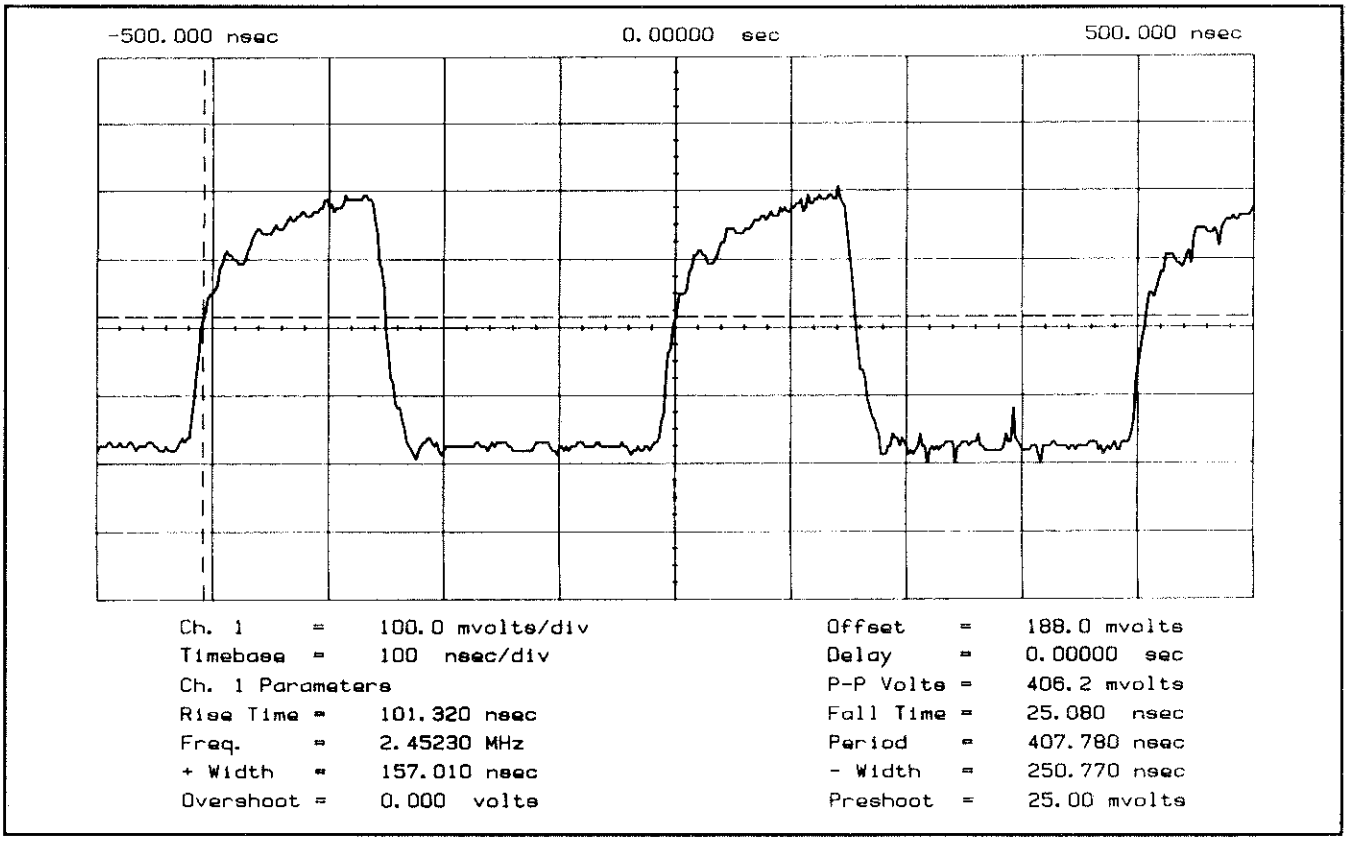


Figure 7G-5. Waveforms at A7U8(6)

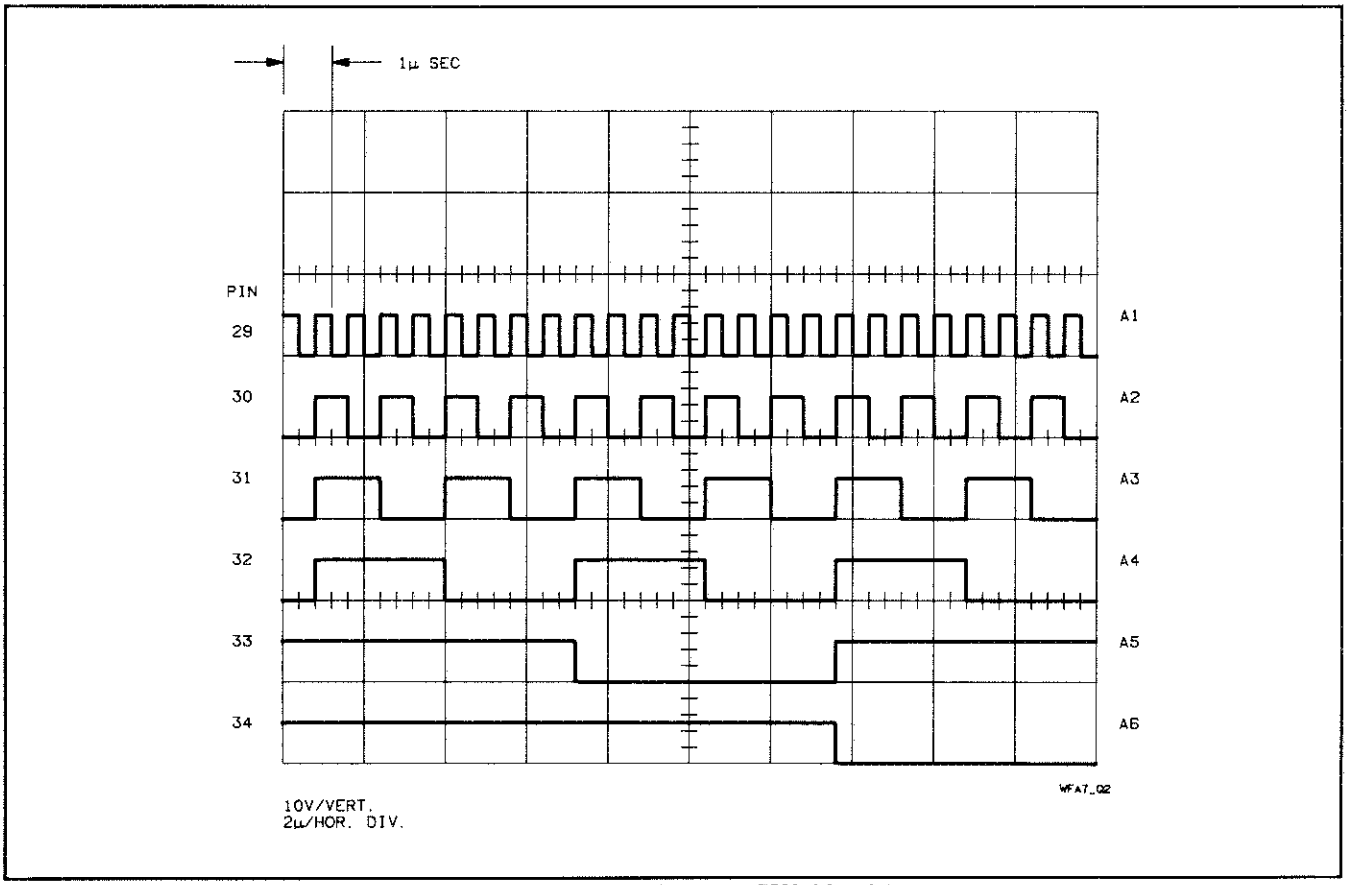


Figure 7G-6. Waveform at A7U8(29 – 34)

Decoding and Buffer Control:

A. Set the board into free-running state (Refer to 68000 Processor paragraph above).

B. Check that A7U14(12-19) goes from +5 V to 0 V every 4 to 5 seconds. Make sure that the sweep rate of the oscilloscope is set as slow as possible. Replace A7U14 if the signals are incorrect and A7U8 functions properly. See *Figure 7G-7.*

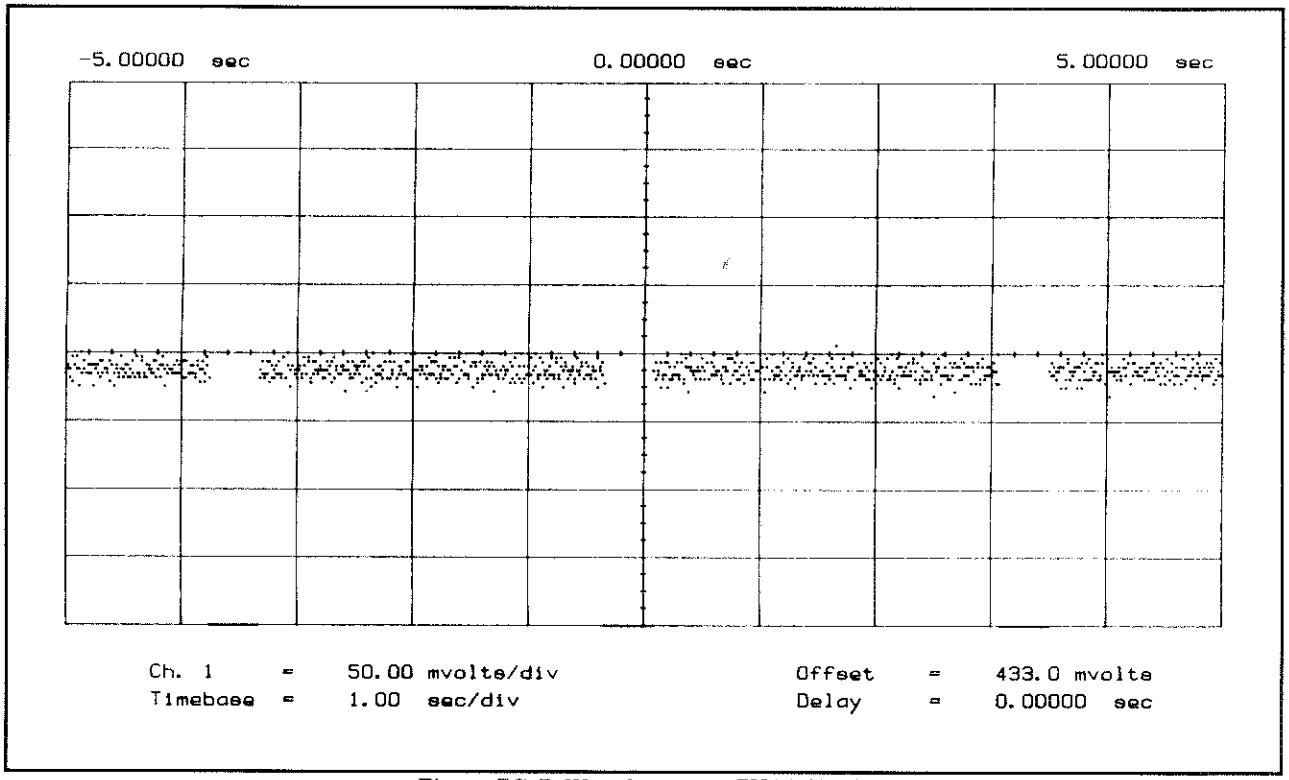


Figure 7G-7. Waveforms at A7U14(12-19)

Global Bus Decoding:

A. Set the board into free-running state (Refer to the 68000 Processor Paragraph above).

B. Check that A7U12(12-15) goes from a 5 V to 0 V every 4 to 5 seconds. If the signals are incorrect, replace A7U12.

Power Down Protection:

Verify that the lithium battery voltage is 3.6 V.

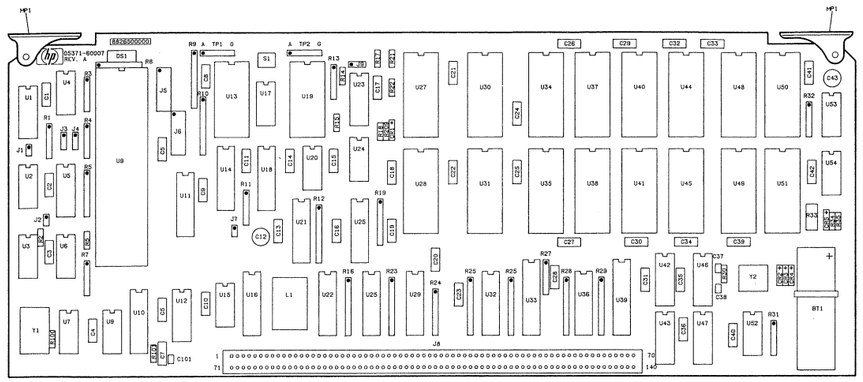
End Of Procedure Steps:

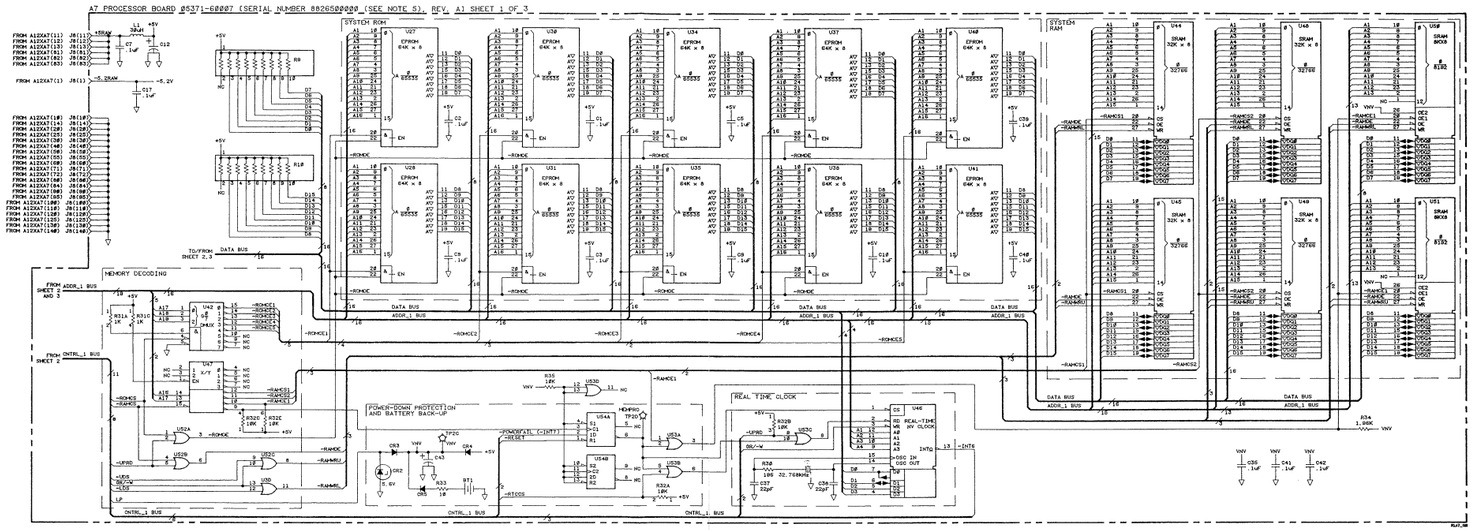
A. Set the jumpers back to their normal positions.

B. Replace the J4 and J2 jumpers.

C. Set the J5 and J6 jumpers in the RIGHT position.

D. Set the J3 jumper to connect the 1st and the 2nd pins.

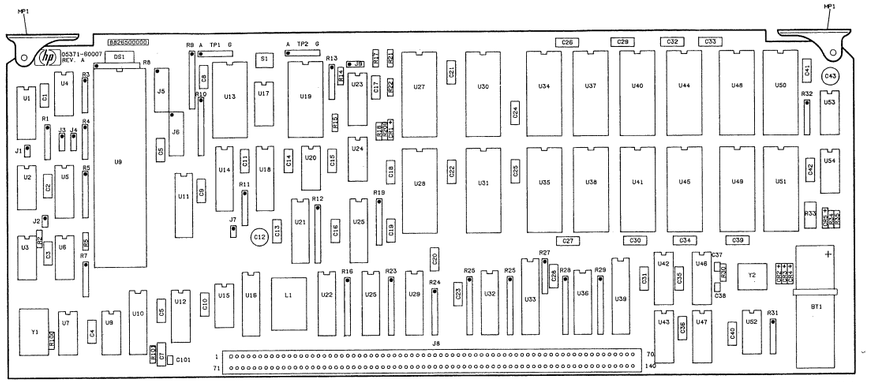




A7 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A7 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

Figure 7G-8. A7 Processor Board Schematic Diagram
(Sheet 1 of 3)



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   INDUCTANCE IN HENRIES.
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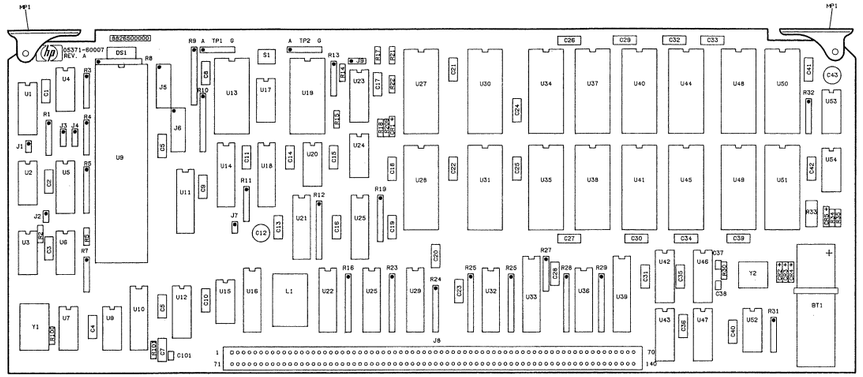
Figure 7G-8. A7 Processor Board Schematic Diagram
(Sheet 2 of 3)



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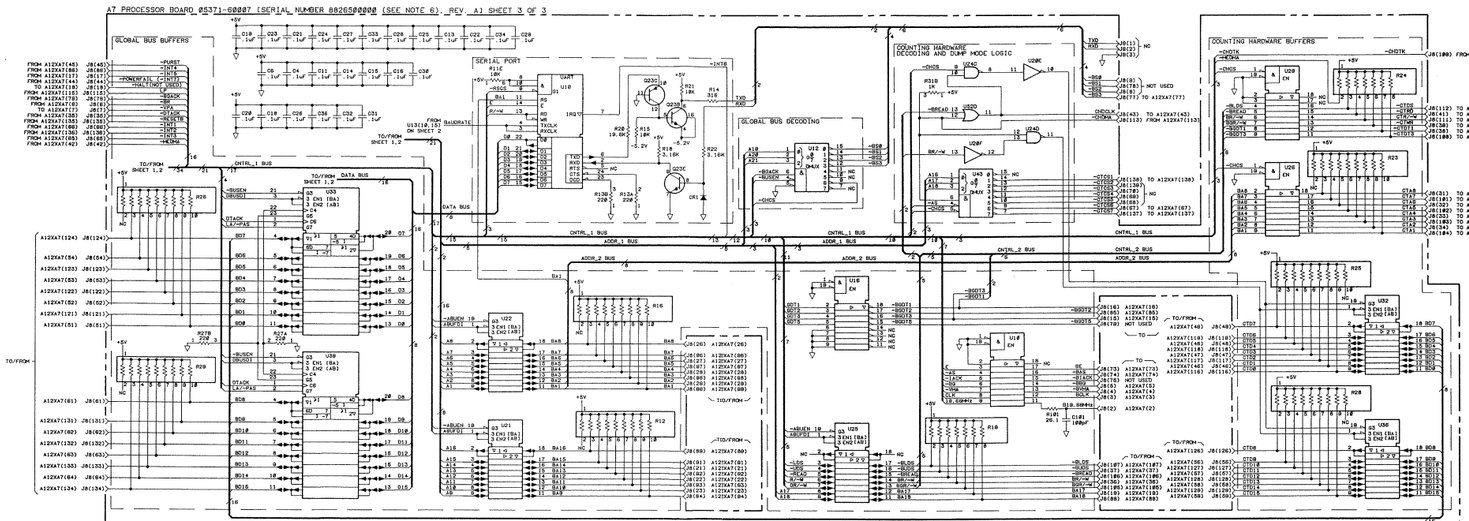


Figure 7G-8. A7 Processor Board Schematic Diagram (Sheet 3 of 3)

SECTION 7H
A8 I/O CONTROLLER BOARD THEORY

7H-1. A8 I/O CONTROLLER BOARD

7H-2. Introduction

The A8 I/O Controller Board and the A7 Processor Board make up the HP 5371A control hardware. The A8 assembly contains the interface circuits to read the front-panel devices, including softkeys, ENTRY/MARKER knob (RPG), and front-panel keypad keys. This board also contains HP-IB interface logic and the DMA circuitry which controls transfer of data from either System or Measurement RAM to the HP-IB. And finally, the CRT memory and control hardware, where bit-mapped CRT images are stored and CRT synchronization and video data signals are generated, are also found on the A8 I/O Controller Board. This boards functions are summarized as follows:

- Provides memory to store a bit-mapped image and the necessary hardware to output it to the A17 CRT Driver Board,
- Provides memory to store measurement data from the A5 ZDT/Count Board Event 1 and Event 2 counter chains,
- Generates synchronization signals for the A17 CRT Driver Board,
- Scans the front panel keyboard,
- Receives and translates signals from the Rotary Pulse Generator (RPG),
- Drives six of the front panel LEDs,
- Handles the HP-IB input and output, and
- Controls direct memory access (DMA) to the HP-IB.

Figure 7H-5 shows the schematic diagram for the I/O Controller Board.

7H-3. CRT Controller Circuit

The CRT Controller Circuit interfaces the 68000 μP and the front-panel CRT display. It provides VIDEO data, Vertical and Horizontal SYNChronization, blanking signal, and address refresh for the *Display Memory*, to the A17 CRT Driver Board. The CRT screen displays an array of picture elements (pixels or dots). Each screen is 408 dots wide by 304 dots high. Each dot can be programmed off, on at half intensity, or on at full intensity (bright). The raster-scan CRT display has an electron beam that starts in the upper-left hand corner, moves across the screen, and then returns to the left-hand edge of the screen. After each such horizontal scan, the beam is incrementally moved down in the vertical direction until it has reached the bottom. At this point, one frame has been displayed, since the electron beam has made 304 horizontal scans and one vertical scan.

For resolution, the characters generated on a frame must be continually repeated. The data to be displayed is stored in four 65K ± 4 bit Dynamic RAMs (A8U15, U19, U23, and U27) by the 68000 μP that controls the system.

The CRT Controller Circuit is comprised of the following circuit blocks:

- CRT Controller (CRTC) IC,
- Display Memory Address Multiplexers,
- Display Timing Generator,
- Display Memory, and
- Video Data Driver.

7H-4. CRT CONTROLLER (CRTC)

The CRT Controller, A8U12, is the interface between the 68000 μP and the raster-scan CRT display. The CRTC contains nineteen programmable registers. These registers are initialized by the 68000 μP via System Data Bus lines BD0-BD7. The 68000 μP programs the CRTC to perform the following functions:

- Generate horizontal synchronization retrace signal (HSYNC),
- Generate vertical synchronization retrace signal (~VSYNC),
- Generate Display Enable (DE) signal which turns off the electron beam during a retrace, and
- Generate 14 horizontal and vertical raster address line (MA0-MA13) output sequence which constantly accesses up to 16K words of bit-mapped video data stored in Display Memory. The process of constantly scanning the address lines also serves to "refresh" all the Dynamic RAM (DRAM) ICs in *Display Memory*.

The bi-directional data bus BD0-BD7 allows the 68000 μP to program the CRTC's nineteen internal registers. The BR/~W line determines if an internal register is to be read from or written to. The register selected is determined by address line BA1 which is connected to the IC's RS pin. When BA1 is low the address register is selected. When BA1 is high the data registers can be accessed. The 68000 μP communicates with the CRTC IC registers by using peripheral control signals E, ~VMA, and ~VPA. When CRTC's address select line, ~SEL0, is enabled (decoded from address lines BA15 through BA18 by decoder A8U36), Valid Peripheral Address (~VPA) line is asserted. The 68000 μP recognizes ~VPA and asserts ~BVMA low. ~SEL0 is ORed with ~BVMA producing CRTC chip select signal ~CRTCCS. The CRTC is now ready for access. The 983 KHz Enable (E) signal synchronizes the data transfer. When the data transfer is completed, the uP disables ~BVMA.

7H-5. DISPLAY MEMORY ADDRESS MULTIPLEXERS

The addressing of DRAM memory locations is accomplished by first sending an 8-bit row address followed by an 8-bit column address. Eight 4-to-1 multiplexers (A8U16, U20, U24, and U28) control this address information sent from either the CRTC or the 68000 μP to the Display Memory. The multiplexers send either row or column address information from either the CRTC or 68000 μP to the *Display Memory*.

7H-6. DISPLAY TIMING GENERATOR

This circuit generates the 9.8304 MHz DOT and 1.2288 MHz CHAR video data clocks and all *Display Memory* timing control signals used in the CRT circuitry. Both clocks and the timing control signals are derived from the buffered 19.6608 MHz system clock provided by the A7 Processor Board. Binary counter A8U4 divides the 19.6608 MHz clock into the following frequencies:

- STATE_A (DOT) 9.8304 MHz
- STATE_B 4.9152 MHz
- STATE_C 2.4576 MHz
- STATE_D (CHAR) 1.2288 MHz

The two clock frequencies, DOT and CHAR, control the output of video data to the A17 CRT Driver Board. The DOT signal shifts video data bits to the CRT display at a 9.8304 MHz rate. The CHAR clock defines the character length (byte) of 8 bits of all data displayed. CHAR operates at a frequency is 1.2288 MHz. STATE_A and STATE_D, which correspond to the DOT and CHAR clock frequencies, are clocked into latch A8U10 at the system clock rate of 19.6608 MHz.

Access to the display memory by the 68000 μP and the CRTC (CRT Controller) is keyed to the CHAR clock signal. This avoids access conflicts between the two. During the first half of the CHAR clock cycle, the 68000 μP has sole access to the display memory. The CRTC can access the display memory only during the second half of the CHAR clock cycle. The 68000 μP is allowed to complete its display memory access only if the ~MEMWAIT signal is asserted low prior to the start of the CHAR clock cycle.

CRT Timing PAL, A8U7, decodes STATE_A through STATE_D to generate signals that control the *Display Memory*. The PAL output signals are as follows:

- ~RAS (Row Address Strobe) — latches the row address into the *Display Memory* DRAM ICs.
- RAS/~CAS (Row and Column Address Strobe) — latches row and column address data into the four-to-one *Display Memory Address Multiplexers*, A8U16, U20, U24, and U28. When signal level is high, the row address is sent to *Display Memory*. If low, the column address is sent.
- ~CAS (Column Address Strobe) — latches the column address into the *Display Memory* DRAM ICs.
- ~MDTACK (~DTACK) — Returned to the 68000 μP upon completion of a memory read or write cycle.
- ~LOAD — instructs the *Video Signal Driver* shift registers to load new data at the next rising edge of the DOT signal.
- ~ENH — Enables the upper byte data buffer, A8U18, that passes data between the *Display Memory* and the 68000 μP. This signal is asserted during a 68000 μP read or write cycle.
- ~ENL — Enables the lower-byte data buffer, A8U26, that passes data between the *Display Memory* and the 68000 μP. This signal is asserted during a 68000 μP read or write cycle.
- ~DTMASK — This signal is used internally by the PAL IC to generate the ~MDTACK signal.

7H-7. DISPLAY MEMORY

Four 65K ± 4 bit dynamic RAMs (A8U15, U19, U23, and U27) store both the bit-mapped representation of the image displayed on the CRT and unprocessed measurement data from the A5 ZDT/Count Board's Event 1 and 2 counter chains awaiting processing by the 68000 μP. The Display Memory is both word-addressable (16 bits at a time) and byte-addressable (8 bits at a time). OR gates A8U13A,B,C, and D produce two write signals, ~WL and ~WH, which separately control the upper and lower bytes of memory. Both write signals are gated by CRT/~MPU, which ensures that they are active only during a 68000 μP access of the *Display Memory*. Since each pixel (or dot) can be in one of three states — off, half-bright, or full-bright — each pixel (or dot) is mapped to two bits within the Display Memory. The lower eight bits of each word corresponds to eight pixels (or dots) of full-bright "plane" of memory. In a similar fashion, the upper eight bits of the same word corresponds to eight pixels (or dots) of the half-bright "plane" of memory. Stored in each "plane" of memory is a separate 408 wide by 304 high pixel (or dot) picture, one displayed at full brightness while the other is displayed at half brightness. When displayed on the CRT, both pictures are superimposed over one another. In other words, bit 0 and bit 8, bit 1 and bit 9, and so on of the same 16-bit word, correspond to the same pixel (or dot) displayed on the CRT.

The addresses sent to the Display Memory are split and time-multiplexed. The row address is sent first followed by the column address. The dynamic RAM needs to have each of its rows refreshed every 4 ms to prevent loss of data. The CRTC performs this "refresh" function by constantly scanning the address lines.

The CRTC drives fourteen address lines capable of accessing 16K words of display memory. Since this CRT Controller is character oriented and can be programmed to display only 128 character rows, two of the address lines are driven by the character row address outputs RA0 and RA1, while the remaining twelve address lines are driven by memory address outputs MA0-MA11. This results in the pixel (or dot) mapping from the CRT display to words in the display memory are not consecutive.

7H-8. VIDEO DATA DRIVER

Two parallel-in, serial-out shift registers (A8U14 and U22) receive video data from *Display Memory* and outputs video data in serial format. Eight bits of video data latch into the shift registers following each CRTC display memory access. Shift register A8U22 is loaded with the lower eight bits of display memory (DT0-DT7) and is displayed by the CRT at full brightness. Shift register A8U14 is loaded with the upper eight bits of display memory (DT8-DT15) and is displayed by the CRT at half brightness. This serial data output is shifted out of the registers at the DOT clock frequency of 9.8304 MHz.

The serial data streams from both shift registers A8U14 and U22 are latched into A8U21 at the DOT clock frequency of 9.8304 MHz. If either serial data stream is present, the VON signal is asserted high. This in turn causes the VIDEO data signal to turn on. The VIDEO data signal can be driven to one of three voltage levels; 0 Volts when the raster is turned off, +2.4 Volts when the raster is on at half-brightness, and +2.6 Volts when raster is on at full-brightness. These voltage levels are set by resistors A8R23, R24, R25, and AND gates A8U25AB. Gate A8U25A turns the raster on and A8U25B, gated by ~VHALF, determines whether the raster is displayed at half- or full-brightness. The signal generated at the output of A8U25A is buffered by an emitter-follower transistor amplifier comprised of A8Q1 and then routed to the A17 CRT Driver Board. When A8U25A output is low, A8Q1 is turned off. When A8U25A output is high, the raster is turned on. The brightness at which the raster is set is now determined by the output of A8U25B. If A8U25B output is set low, the brightness of the raster decreases as more current is pulled through A8R23.

A8U21 and U21 also latch the VDE and ~MEMWAIT lines. VDE, the display disable line, is active only between raster retraces. This signal originates at the CRTC, as DE, and is latched into A8U8, synchronizing it with VIDEO data output. VDE gates the VON and ~VHALF signals. When VDE is low, the CRT display is blank. ~MEMWAIT signal indicates that the 68000 μP is waiting to access the *Display Memory*.

7H-9. Microprocessor Interface

This circuitry serves the following two functions:

- A8U36 and U42 decodes System Address lines BA15-BA18 to generate miscellaneous chip select, enable, and clock signals for ICs located on the A8 I/O Controller Board, and

- A8U40 and U44 generate the System Bus Data Transfer ACKnowledge signal (~DTACK).

A8U36 and U42 decode System Address lines BA15-BA18 to generate the following IC selection signals:

Table 7H-1. IC Selection Signals

Signal	Description
~SEL0	CRT Controller (A8U12) Chip Select
~SEL1	Keyboard Controller (A8U1) Chip Select
~SEL2	LED Latch (A8U9) Enable
~SEL3	HP-IB Controller (A8U50) Chip Enable
~SEL4	DMA Address Latch (A8U33) Clock
~SEL5	DMA Controller (A8U30) Chip Select
~SEL6	DMA Interrupt Clear (A8U25D)
~SEL7	DMA Byte Latch (A8U43) Enable
~SELM	Indicates 68000 uP awaits access to Display Memory

A8U40ABCD and U44ABCD outputs are wire-ORed together to generate the System Bus Data Transfer ACKnowledge (~DTACK) signal signal which indicates to the 68000 μP that a read or write has been successfully completed and that the microprocessor can end the current bus cycle.

7H-10. Front Panel Control Circuitry

The Keyboard Controller IC, A8U1, scans the front panel keyboard and the Rotary Pulse Generator (RPG). A8U1 scans the front panel by manipulating an 8-to-1 multiplexer (A8U2) and a BCD-to-Decimal decoder (A8U3). The BCD-to-Decimal decoder successively pulls each keyboard row scan line low one at a time. While each scan line is low, each column scan line is returned to the Keyboard Controller (A8U1) for testing via the 8-to-1 multiplexer (A8U2). Pressing a front panel key is detected when a low signal is detected on the return line.

The Keyboard Controller IC also checks the RPG for rotation by checking the state of the RPG Input Circuitry (A8U5 and U32). Two signals, RPG1 and RPG2, are generated by the RPG whenever the front panel ENTRY/MARKER knob is rotated. These signals are 90 degrees out of phase from one another. When the RPG is rotated clockwise, the RPG2 leads RPG1 by 90 degrees. Conversely, when the RPG is rotated counterclockwise, RPG2 lags RPG1 by 90 degrees. Both signal pulse at the rate of 120 pulses per revolution. The RPG1 and RPG2 signals are routed from the RPG, which is mounted on the front panel (labeled ENTRY MARKER, to two inverting buffers mounted on the A8 I/O Controller Board. Both signals are then routed to flip-flop A8U5 whose function is to determine when a CLICK pulse has occurred and in what direction the RPG was rotated when the DIR pulse occurred. The Keyboard Controller A8U1 periodically polls the A8U5 flip-flops for activity. After polling is complete, the BCD-to-Decimal decoder A8U3 clears flip-flop A8U5A via ~CLICK CLEAR signal.

When the Keyboard Controller IC (A8U1) detects a front panel key depression or an RPG (labeled ENTRY/MARKER) rotation, it generates a 68000 μP interrupt, ~INT5. At the end of the current bus cycle, the 68000 μP reads the data from A8U1 via System Data Bus lines BD0-BD7. The interrupt generated, ~INT5, is automatically cleared when data is read from the Keyboard Controller's data line outputs.

7H-11. LED Control Circuit

An eight-bit register (U6) drives six front panel LEDs: A11DS1 ("RMT"), A11DS2 ("LSN"), A11DS3 ("TLK"), A11DS4 ("~SRQ"), A11DS5 ("GATE"), and A11DS6 ("SINGLE"). The anodes of these diodes connect to +5 Vdc on the A11 Front Panel Board. The diode cathodes connect to A8U6 outputs through current-limiting resistors, which are mounted on the A8 I/O Controller Board. A8U6 outputs are inverted so that when a logical "1" is latched in, the output is pulled low and an LED lights. The outputs of A8U6 are also connected to inverted bus driver A8U9. A8U9 allows the 68000 μP to read the state of the LEDs over the System Data Bus (BD0-BD7).

7H-12. 5 MHz Clock Driver

Flip-flop A8U11B is configured to divide the 9.8304 MHz clock (BCLK) from the A7 Processor Board into two 4.9152 MHz signals. These two signals, 5MHz and ~5MHz supply clock inputs to the Front Panel Controller (A8U1), the HP-IB Controller (A8U50), and the DMA Controller (A8U30).

7H-13. HP Interface Bus Control Circuit

7H-14. GENERAL BUS DESCRIPTION

The Hewlett-Packard Interface Bus (HP-IB) is a carefully defined instrumentation interface which simplifies the integration of instruments, calculators, and computers into systems. It minimizes compatibility problems between devices and has sufficient flexibility to accommodate future products. The HP-IB is Hewlett-Packard's implementation of IEEE Std 488-1978 "Standard Digital Interface for Programmable Instrumentation".

The HP-IB employs a 16-line bus to interconnect up to 15 instruments. This bus is normally the sole communication link between the interconnected units. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight of the lines are used to transmit data and the remaining eight are used for communication timing (Handshake), and control.

Data is transmitted on the eight HP-IB data I/O lines, ~DIO1-~DIO8, as a series of eight-bit characters referred to as bytes. Each character byte transferred on the HP-IB data lines employs the three-wire handshake sequence. This sequence has the following characteristics:

A. Data transfer is asynchronous — Data can be transferred at any rate suitable for the devices operating on the bus.

B. Devices with different input/output speeds can be interconnected. Data transfer rate automatically adjusts to slowest active device.

C. More than one device can accept data at the same time.

Communication between devices on the HP-IB employs the three basic functional elements listed below. Every device on the bus must be able to perform at least one of these functions:

A. LISTENER — A device capable of receiving data from other instruments. When addressed to LISTEN, the 5371A will accept any number of commands from the external controller. These commands program the 5371A operation. Several listeners can be active simultaneously.

B. TALKER — A device capable of transmitting data to other instruments. At its simplest level, the 5371A can transmit data in the "talk only" mode to output devices such as a printer or plotter. In more sophisticated systems, the external controller can program the 5371A to perform a specific type of measurement and direct it to process and transfer the results. The 5371A can be addressed to TALK by the external controller or by setting the instrument to the TALK ONLY mode. Only one talker can be active at a time.

C. CONTROLLER — A device capable of managing communications over the HP-IB, such as addressing and sending commands. The 5371A cannot be used as a controller.

An HP-IB system allows only one device at a time to be an active talker. Up to 14 devices may simultaneously be listeners. Only one device at a time may be an active controller.

7H-15. HP-IB SIGNALS

The eight data I/O lines, ~DIO1-~DIO8, are reserved for the transfer of data and other messages in a byte-serial, bit-parallel format. Data and message transfer is asynchronous and is coordinated by three handshake lines: Data Valid (~DAV), Not Ready for Data (~NRFD), and Not Data Accepted (~NDAC). The other five lines are for management of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The active controller manages all bus communications. The state of the ATN (attention) line, determined by the controller, defines how data on the eight data (DIO) lines will be interpreted by the other devices on the bus. When ATN is low (true), the HP-IB is in Command Mode. In Command Mode, the controller is active and all other devices are waiting for instructions. Command Mode instructions that can be issued by the Controller in "Command Mode" include:

A. Talker Address — A seven-bit code transmitted on the HP-IB that enables a specific device to talk. Only one bus device at a time may act as the talker. When the controller addresses a unit to talk, the previous talker is automatically unaddressed and ceases to be a talker. Confusion would result if more than one device were allowed to talk at a time.

B. Listener Address — A seven-bit code transmitted on the HP-IB that enables a specific device to listen. Several bus devices at a time (up to 14) may be listeners.

C. Universal Commands — Bus devices capable of responding to these commands from the controller will do so at any time regardless of whether they are addressed. These commands will be covered in more detail later.

D. Addressed Commands — These commands are similar to Universal Commands except that they are recognized only by devices that are addressed as listeners.

E. Unaddress Commands —

1. "Unlisten" Address Command — This command unaddresses all listeners that have been previously addressed to listen.

2. "Untalk" Address Command — This command unaddresses any talker that had been previously addressed to talk.

When ATN (attention) goes high (false), the HP-IB is in the "Data Mode". In this mode, data may be transferred between devices that were addressed when the HP-IB was in "Command Mode". Messages that can be transferred in "Data Mode" include:

A. Programming Instructions – Codes are seven- (or eight-) bit bytes placed on the HP-IB data (DIO) lines. The meaning of each byte is device dependent and is selected by the equipment designer. These types of messages are usually between the controller, acting as the talker, and a single device that has been addressed as listener.

B. Data Codes – Data codes are seven- (or eight-) bit bytes placed on the data lines. The meaning of each byte is device dependent. For meaningful communication to occur, both the talker and listener must agree on the meaning of the codes they use.

The 68000 μP reads the device address of the HP 5371A from non-volatile memory and writes it to the HP-IB Controller IC. The default value of the device address is "3", but values between 0 and 30 can also be selected from the front panel SYSTEM Menu screen. While the ~ATN is true, all devices must listen to the data lines. When the ~ATN line is false, only devices that have been addressed will actively send or receive data; all others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is placed on the data lines (while ~ATN is true), all other talkers are automatically unaddressed. Information is transmitted on the data lines under sequential control of the ~DAV, ~NRFD, and ~NDAC handshake lines. No step in a sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than the slowest device presently addressed as active. This permits the several devices to receive the same message byte simultaneously.

The ~ATN is one of the five management lines. When ~ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII codes. When ~ATN is false, and code of 8 bits or less understood by talker and listener(s) may be used. The Interface Clear (~IFC) line places the interface in a known quiescent state via the abort message. The Remote Enable line (~REN) is used with the remote, local, and clear lockout/set local message to select either local or remote control of each device. Any active device can set the Service Request (~SRQ) line true. This indicates the need of the sending device for attention by the controller. The End or Identify line indicates the end of a multiple-byte transfer sequence when set low. When the controlling device sets both the ~ATN and the ~EOI lines true, each device capable of a parallel poll, which the HP 5371A is not, indicates its current status on the DIO line assigned to it.

7H-16. HP-IB CIRCUIT COMPONENTS

HP-IB Controller, A8U50, interprets HP-IB commands and controls the direction of data flow from an external to the System Bus. A8U50 communicates via thirteen internal memory mapped registers. Six of the registers are read only, and seven are write only. All communication between the HP-IB port and the 68000 μP is handled by these registers. System address line bits, BA1-BA2, which connect to register select lines RS0-RS2, are used to select a particular register. A low on ~SEL0, the IC's chip enable line, indicates that the 68000 μP is performing either a read or write from a selected register. BR/~W, connected to the IC's DBIN pin, specifies whether a read or write is being performed. A high indicates a 68000 μP read. When both the BR/~W and ~HPIBWR (WE) are set low, the 68000 μP writes to a selected IC register. Data transfer occurs over eight bi-directional System Data Lines, BD8-BD15.

The HP-IB Controller Interrupt line, ~INT4, indicates to the 68000 μP that A8U50 requires servicing. This interrupt is processed by 68000 μP which jumps to a service subroutine at the end of the current bus cycle.

All of the input/output signals from the HP-IB Controller IC, A8U50, are routed through two bi-directional bus management transceivers, A8U47 and U48. These two devices are controlled by CONT (CONTroller), TE (Talk Enable), ~ATN (Attention) and ~EOI (End or Identify). A8U48 controls the direction command and data transfer signals. The direction of the command signals ~ATN, ~SRQ, ~REN, and ~IFC is determined by the ~CONT signal. The direction of data transfer control signals ~DAV, ~NRFD, and ~NDAC is controlled by the TE signal. The direction of data byte flow through transceiver A8U47 is controlled by TE, ~ATN, and ~EOI. Both transceivers' outputs satisfy IEEE-488 standard termination requirements. When power is removed from the either transceiver, all outputs present a high impedance to the bus.

When operating in DMA mode, the HP-IB Controller IC (A8U50) performs fast transfers of data blocks from either count hardware or 68000 μP memory through the HP-IB port using the ~ACCRQ (DMA Request) and ~ACCGR (DMA Grant) handshake lines. See *DMA Control Circuit* theory for more details.

7H-17. Bus Arbitration Circuit

ICs A8U41D, U45AB, U46B, and U49A provide decoding for the signals required by the DMA Controller IC, A8U30, and the 68000 μP, A7U8, during the arbitration process for control of the bus system. Prior to any transfer of data by the DMAC, (A8U30), it must gain control of the bus from the 68000 μP. The arbitration process is initiated by the DMAC when it sets the HREQ signal high. This sets the 68000 μP Bus Request signal (~BR) low. When the 68000 μP is ready to relinquish its control of the bus, it sets the 68000 μP Bus Grant signal (~BG) low. The DMAC can now take control of the bus when the following four processes have occurred:

- ~BG is received,
- Address strobe (~AS) is inactive, indicating that the 68000 μP is not using the bus,

- ~DTACK is inactive indicating that neither memory nor peripherals are using the bus, and
- Bus Grant Acknowledge (~BGACK) is inactive which indicates that no other control device is laying claim to the bus.

The Bus Grant Acknowledge line, ~BGACK, is asserted low when the previous conditions are met. In response the 68000 μP sets the Bus Request, ~BR, low causing it to relinquish control of the bus to the DMAC.

When the DMAC is finished using the bus, it releases control by clearing HREQ. The 68000 μP responds by setting the Bus Grant Acknowledge line (~BGACK) high.

7H-18. DMA Control Circuit

The heart of the DMA Control Circuit is the Direct-Memory-Access-Controller (DMAC), A8U30. The DMAC controls the high speed transfer of one or more data words between the count hardware memory or 68000 μP memory and the rear-panel HP-IB port. The DMAC generates the 16-bit 68000 μP memory addresses ("System RAM") and the memory READ signals during transfer of processed data (ASCII or floating point) from memory. It also controls how many memory locations are accessed during each DMA cycle. When transferring unprocessed binary data, DMAC operation is similar except that the measurement RAM addresses are generated by the A6 DMA/Gate Board's "DMA Measurement RAM Address Generation" circuit. (The 16-bit address generated by DMAC during a binary dump is not used.) The rate at which data is transferred to an external controller depends on both data format (i.e., ASCII, Floating Point, or Binary) and type of measurement data (i.e, Frequency A, Period A, etc.). (Refer to *Table 1-1*, HP 5371 Specifications, for characteristic measurement output rate information.)

The DMA Controller performs the following types of data transfers:

- Transfer of unprocessed binary data directly from the count hardware memory located on the A5 ZDT/Count and A6 DMA/Gate Boards directly to the HP-IB,
- Transfer of processed data (i.e., ASCII or floating point data, Timing Counter ZDT chain results) from the A7 Processor Board's *System Ram* directly to the HP-IB, and
- Transfer of processed Event Counter 1 and 2 measurement data from the A8 I/O Controller Board's *Display Memory* directly to the HP-IB.

The following paragraphs describe a typical DMA transfer.

A. Prior to DMA transfer, the 68000 μP loads the starting memory address of data to be transferred into DMAC's address register, and the number of data bytes to be transferred into DMAC's terminal count register. The 68000 μP selects the DMAC's internal registers via bidirectional address lines BA1-BA3. Data is loaded into DMAC via bidirectional data lines DB0-DB7 when ~SEL5 line is asserted (low). In binary mode, only the number entered into the terminal counter is used. The address provided by DMAC is not used since all count hardware memory addressing is controlled by the A6 DMA/Gate Board.

B. The DMA Register, A8U33, stores upper address bits BA16-BA18 from System Data bus lines BD0-BD7. During a DMA transfer, the BA16-BA18 bits are buffered from the System Data Bus by A8U37 and placed on the Control Bus (CNTRL BUS). These address bits, sent to the A7 Processor Board's Address Decode PAL (A7U14) and "Memory Decoding" circuit for decoding, are used for memory IC selection. Data stored in the DMA register also determines whether counting hardware memory (~CHDMA asserted) or 68000 μP memory (~MEDMA asserted) is accessed during a DMA transfer, and whether a DMA interrupt (~INT4) is enabled or disabled.

C. After the HP-IB Controller IC, A8U50, has been configured as a talker and the external controller is ready to receive data (TE and ~NRFD are asserted), it sends a service request, DREQ1 (Dma REQuest

1), to the DMAC. This informs the DMAC that the HP-IB Controller is ready to transfer a byte of data.

D. After the DMAC receives DREQ1, it forwards this request to the 68000 μP by asserting its HREQ (Hold REQuest) line. HREQ is routed to the "Bus Arbitration Circuit" where the ~BR (Bus Request) line is asserted. ~BR is sent directly to the 68000 μP.

E. After sensing the ~BR low, the 68000 μP finishes its current bus cycle and asserts (low) its ~BGACK (Bus Grant ACKnowledge) line. ~BGACK is routed to the "Bus Arbitration Circuit" where the HACK (Hold ACKnowledge) is asserted. HACK is sent directly to DMAC. The 68000 μP enters a wait state and releases control of the address and data buses.

F. The DMAC senses HACK and forwards the acknowledge signal, ~DACK1 (Dma ACKnowledge) to the HP-IB Controller IC, informing it that 68000 μP activity has been suspended and that the DMA transfer may proceed.

G. The DMAC loads the starting memory address on the address bus; BA1-BA7 are loaded directly while BA8-BA15 are sent to Address Latch, A8U35, via bidirectional data lines DB0-DB7. A8U35 drives address bus lines BA8-BA15 during a DMA transfer. The DMAC, A8U30, writes data to A8U35 when address strobe line ADSTB is set high.

H. The DMAC now supplies the memory being accessed with the appropriate read and write signals. This signals are the ~BR/~W, BGR/~W, and ~BREAD are duplicates of the signals generated by the A7 Processor Board during non-DMA data read/write cycles.

I. The HP-IB Controller IC can now transfer 16-bit data words from a specified memory to the HP-IB port, one byte for each DREQ1/~DACK1 handshake sequence. During each handshake sequence, the DMA Controller takes control of the data bus and transfers a single byte of data, and then relinquishes control of the data bus back to the 68000 μP. This ensures that the 68000 μP has access to the bus should the HP-IB port malfunction.

J. After each byte transfer, DMAC increments its internal address register and terminal count register.

K. When the DMAC has finished a programmed DMA dump, its End of Process line, EOP, is set high. This causes flip-flop A8U11A and inverter A8U41B to assert ~INT4, assuming that the interrupt was not disabled by line ~INT_DISABLE.

7H-19. DMA Byte Latch

A8U43, the DMA Byte Latch, stores the lower byte of each data word read by the DMA Controller. Since the HP-IB Controller (A8U50) accommodates only 8-bit bytes and the A5 ZDT/Count count hardware outputs only 16-bit words, the upper 8-bit byte is read directly by the HP-IB Controller while the lower 8-bit byte is stored by the DMA Byte Latch. During the next DMA cycle, no data will be read from memory and the data stored in the DMA Byte Latch is now read by the HP-IB Controller. The logical state of address line A0 from the DMA Controller, A8U30(32), determines whether a word is read from memory (BA0 = 0) or if an 8-bit byte is read from the DMA Byte Latch (BA0=1).

7H-20. A8 Troubleshooting Procedure

The A8 board should be checked if any of the following symptoms occur:

- The CRT does not provide the correct display
- Counter does not respond to instructions from the front panel

- Counter has trouble communicating with a computer or other peripheral devices
- The LED indicators on the front panel malfunction

A. Before troubleshooting any part of the circuit, observe that a 5 MHz signal exists at A8U11(9).

B. If the signal does not exist, verify that the A12 board supplies a 10 MHz signal to A8U11(11) and that A8U11 functions properly.

7H-21. CRT Controller Circuit

The CRT controller circuit should be checked if the CRT does not provide the correct display.

7H-22. Display Timing Generator

A. Verify that a 20 MHz signal exists at A8U10(9) as shown in *Figure 7H-1*. If not, check the A1 board.

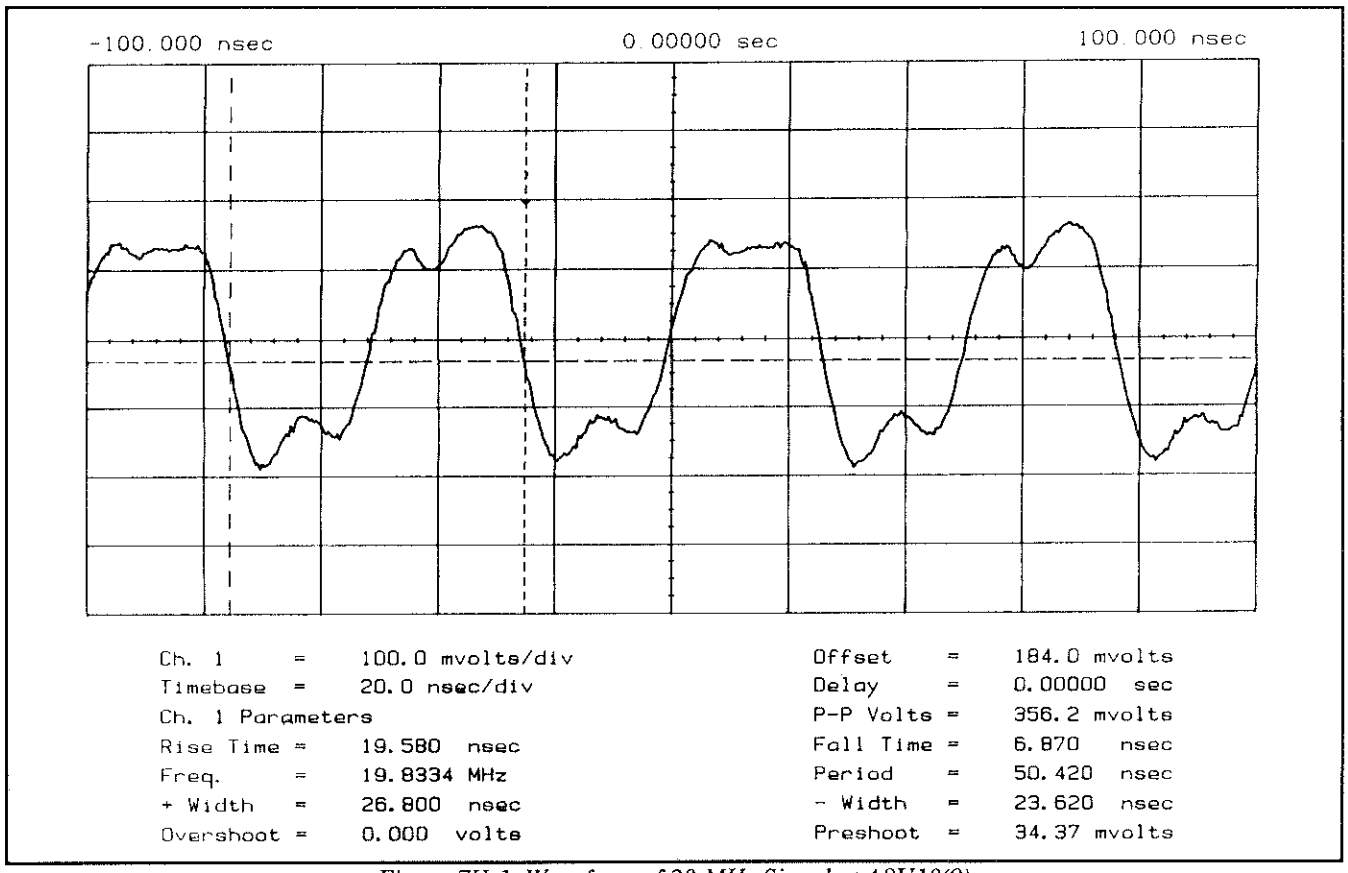


Figure 7H-1. Waveform of 20 MHz Signal at A8U10(9)

B. Check that A8U7(2) and A8U7(5) display a 9.83 MHz and a 1.23 MHz respectively. If the signals are not present, make certain that A8U4(1), the clear signal, is not low. If the clear signal is low, replace A8U4. Otherwise, check the end of R10 that is connected to +5V.

7H-23. CRT Controller

A. Verify that the CRTCCS signal at A8U12(25) is high. If it is low, then replace A8U34 which generates the signal. If the problem persists after A8U34 has been replaced, check the A12 motherboard.

B. Probe A8U12(39) and A8U12(40). (These are the HS and VS signals.) Compare them with *Figures 7H-2* and *7H-3*. If either is incorrect, replace A8U12.

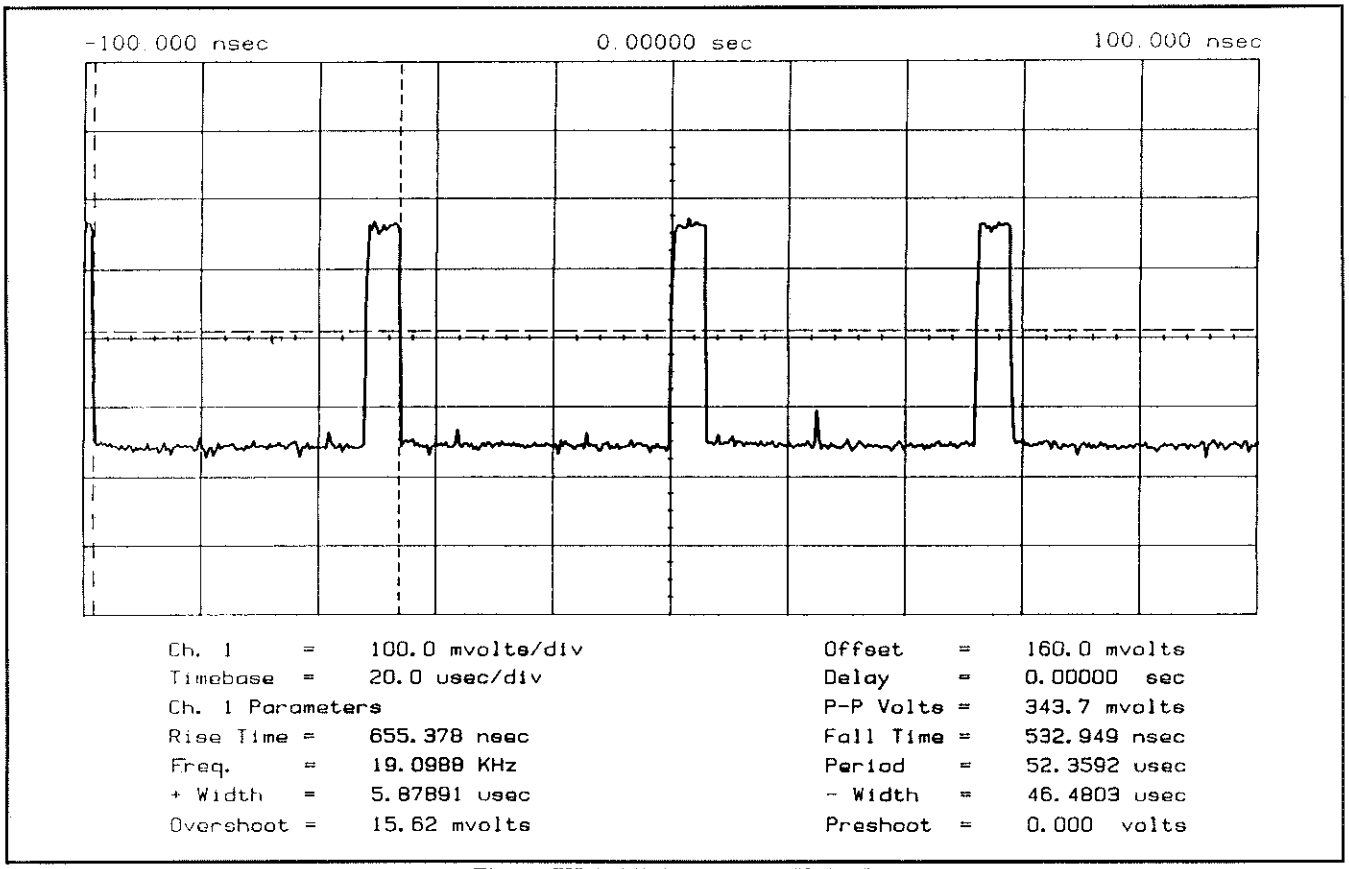


Figure 7H-2. HS Signal at A8U12(25)

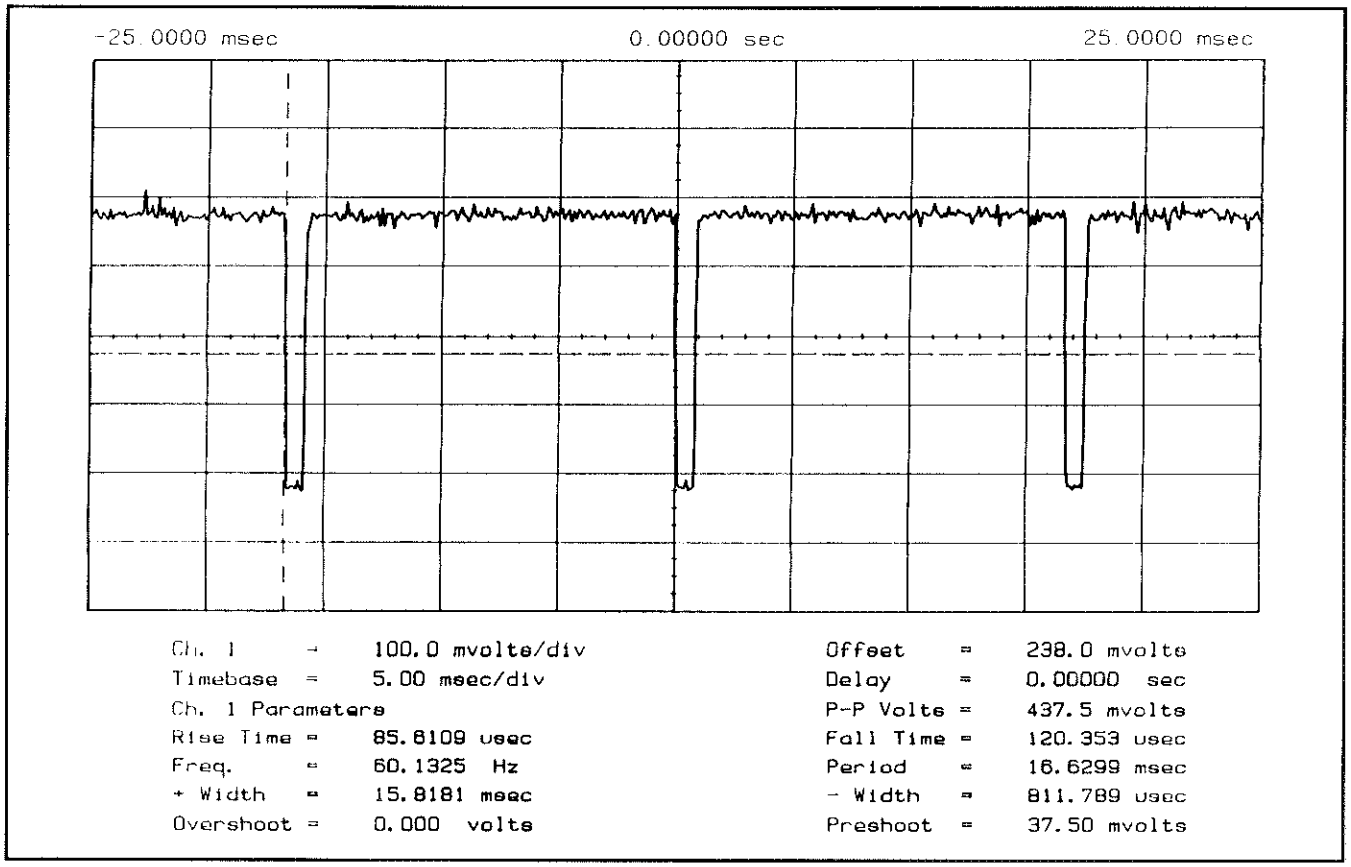


Figure 7H-3. VS Signal at A8U12(40)

7H-24. Video Signal Driver

A. Verify that A8U14(13), the output of the parallel-in serial-out circuit, and A8U14(2-14), the input of U14, toggle at TTL-levels.

B. If both signals are present, then proceed to the step O. Otherwise, verify that A8U14(15), the load signal, toggles at a frequency of approximately 1 MHz. See *Figure 7H-4*.

C. If A8U14(15) is correct and A8U14(13) is incorrect, then replace A8U14.

D. Repeat Steps A through C for U22.

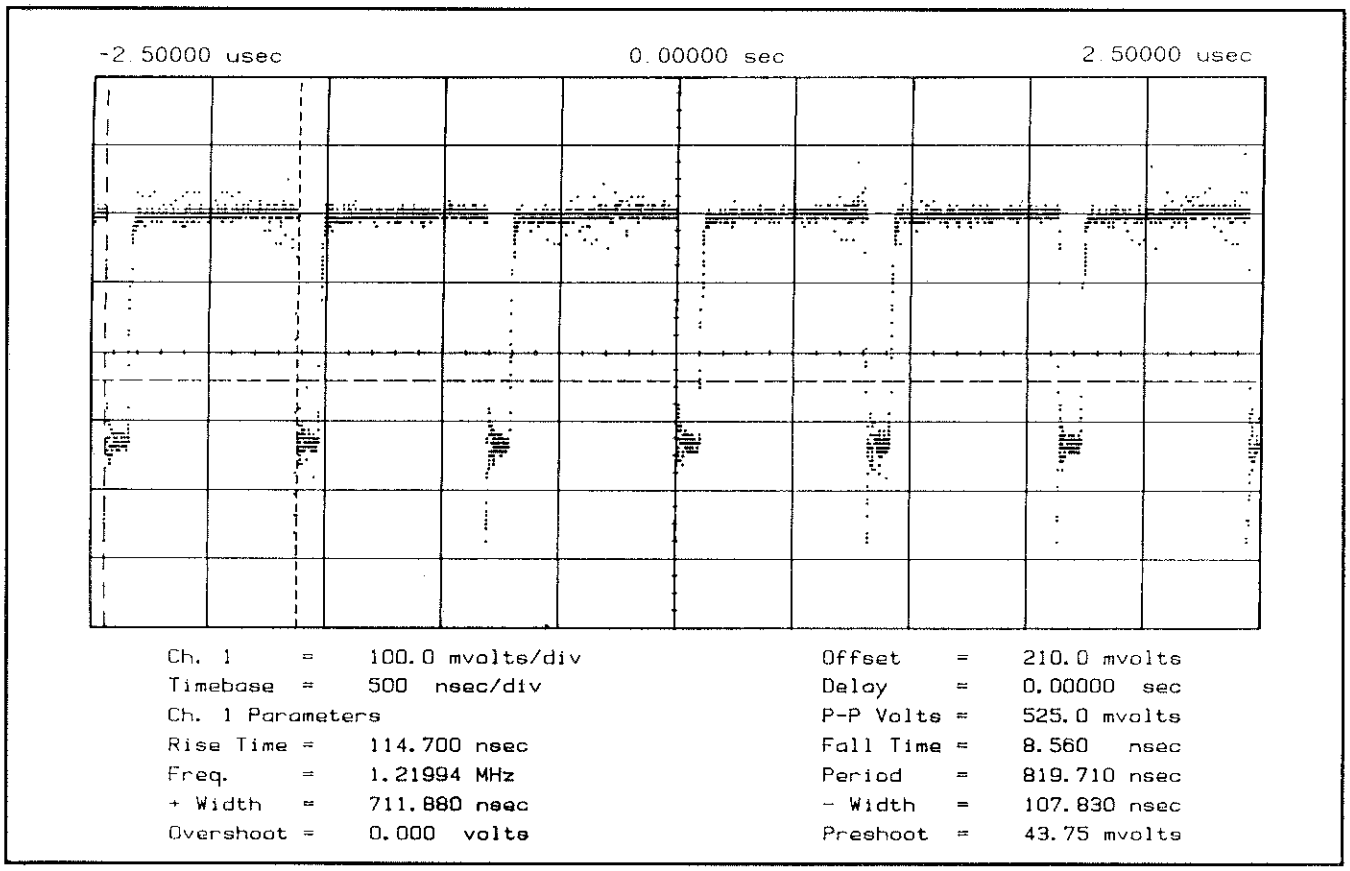


Figure 7H-4. 1MHz Signal at A8U14(15)

7H-25. Front Panel Control Circuitry

A. Verify that the RPG1 and RPG2 pulses are present at A8U32(1) and A8U32(3) when the MARKER knob at the front panel is turned. If the pulses are not present, check the A11 board.

NOTE

A convenient method to observe the signal is to set the scope to a high sweep rate and large voltage per division, then continue to turn the RPG knob to generate a signal.

B. Check that A8U1(6), the chip enable for the CRT Controller, is high. If the signal is low, check the A12 and the A7 boards.

C. Verify that A8U12(30) toggles. If the signal is incorrect, replace U1 the KBD Controller.

D. Observe that A8U3(3) is low. If it is high, the BCD-DEC converter is faulty, therefore, replace A8U3.

7H-26. HP-IB Circuitry

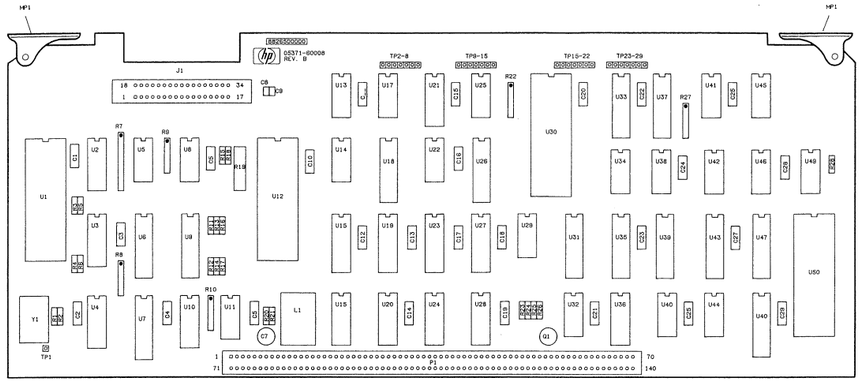
A. Make sure that the HP-IB cable is connected securely to the HP 5371's rear panel HP-IB connector. and to the external device. Check that the addresses of all devices are correct.

B. If the HP 5371A has problems in communicating with other devices, then replace A8U50.

7H-27. LED Control Circuitry

A. Verify that A8U17(11), the LEDWR signal, is high. Otherwise, check A8U17 and the A7 board.

B. Verify that A8U6, a positive-edge triggering, type D Flip-flop, and the LED, both function properly. If not, replace A8 and/or the faulty LED(s).



A8 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A8 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

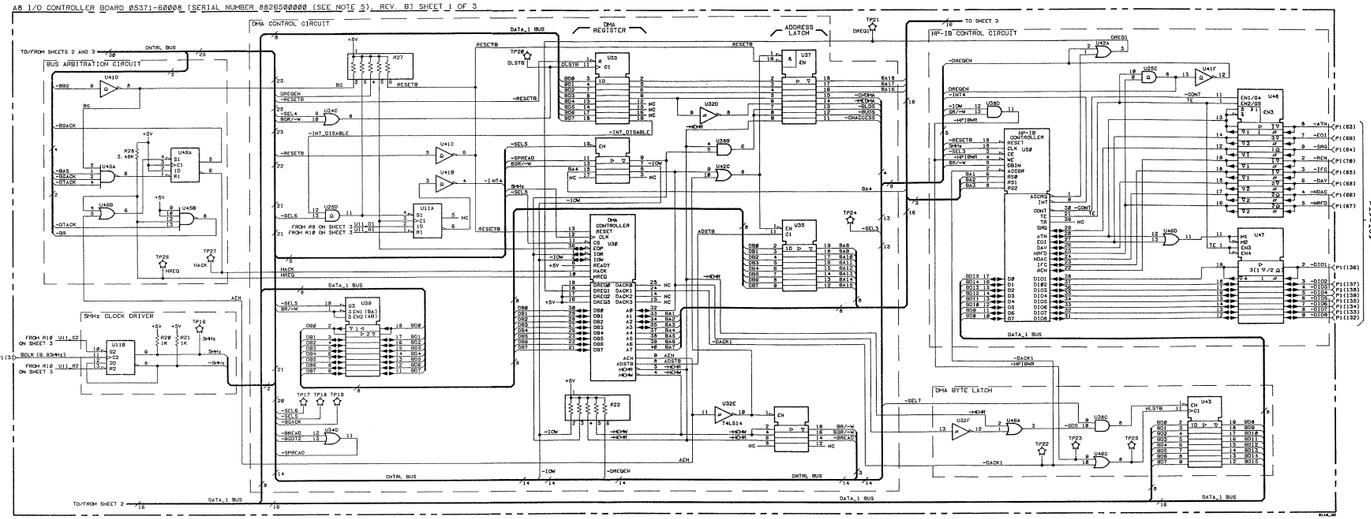
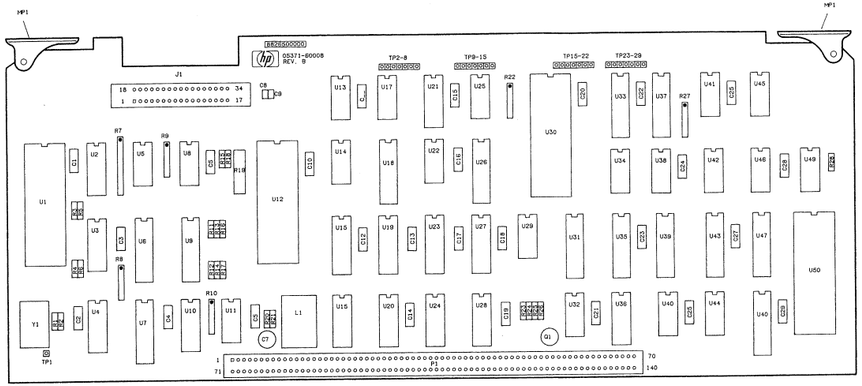


Figure 7H-5. A8 I/O Controller Board, Schematic Diagram
(Sheet 1 of 3)



A8 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A8 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
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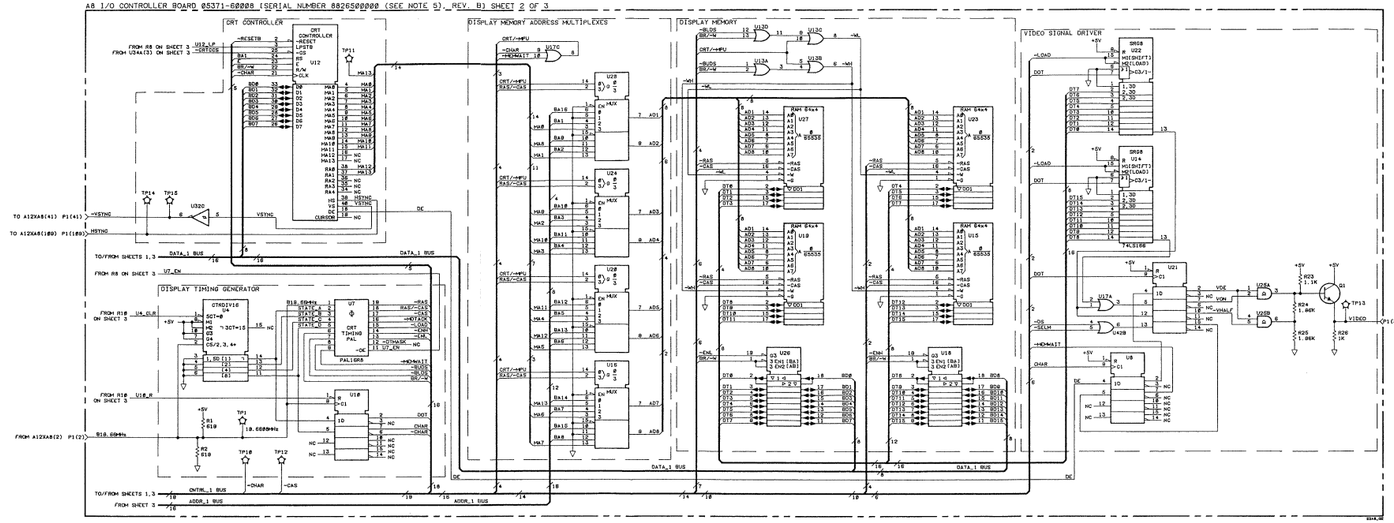
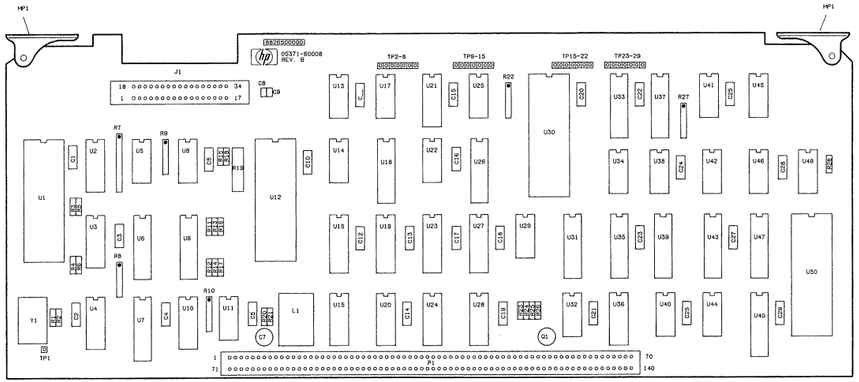


Figure 7H-3. A8 I/O Controller Board, Schematic Diagram (Sheet 2 of 3)



A8 SCHEMATIC DIAGRAM NOTES

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3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
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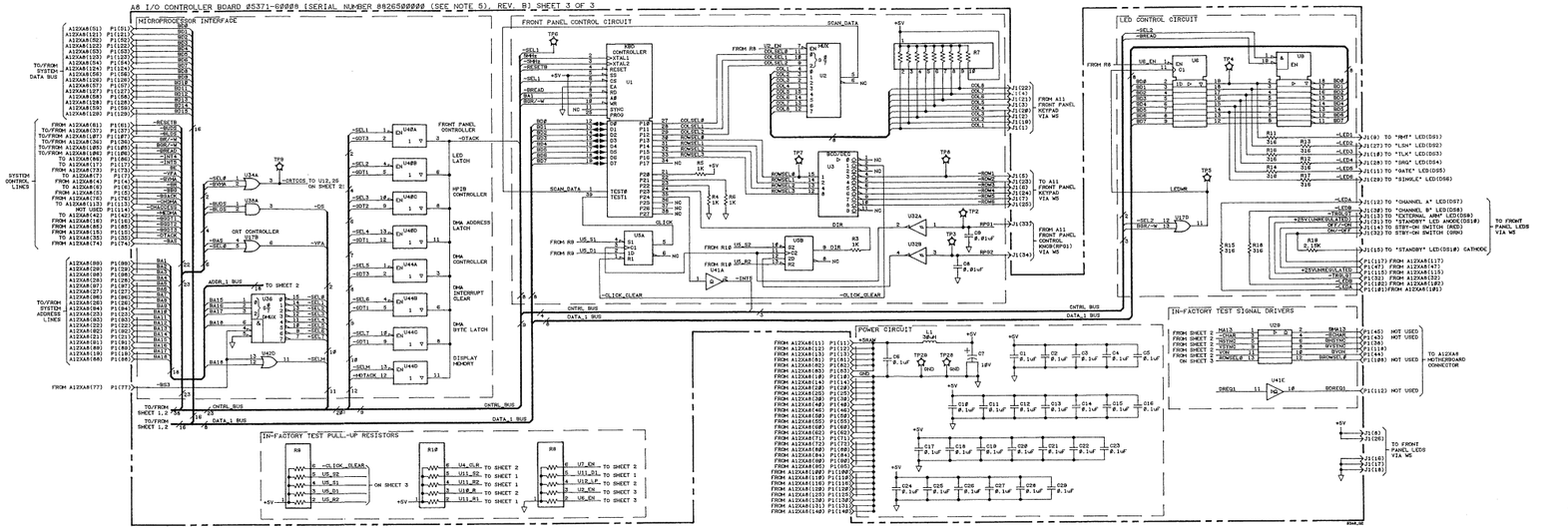


Figure 7H-3. A8 I/O Controller Board, Schematic Diagram (Sheet 3 of 3)

71 POWER SUPPLIES

SECTION 7I
POWER SUPPLIES

7I-1. A9 DOUBLE REGULATOR BOARD

The schematic diagram for A9 is shown in *Figure 7I-1*. The A9 Double Regulator provides –5.2 Vdc (for ECL circuits) from a switching supply and –3.3 Vdc (for EFL circuits) from a linear supply. The linear –3.3 Vdc supply is driven from the –5.2 Vdc supply output. Both supplies are protected by 10-amp fuse A9F1.

7I-2. –5.2 Volt Regulator

Pulse width modulator A9U1 turns on A9Q1 via A9Q2 and Q4, which applies a fixed voltage across inductor A9L3. When A9Q1 is off, the energy stored in its magnetic field is transferred to capacitors A9C12 and C14 and to the applied load through diode A9CR3. A9C12 and C14 supply most of the current to the load when A9Q1 is forward biased and A9CR3 is reversed biased. A9U1 operates at a nominal switching frequency of 40 kHz.

When the HP 5371A is first powered up, a "soft" start is provided by limiting the pulse width output of A9U1 until capacitor A9C4 is fully charged. When the front-panel STBY-ON switch is in the STBY position, the +25V unregulated voltage remains energized while the +5V and the –15V supplies are de-energized. The –5.2V power supply will not operate until the +5V supply (located on the A10 Triple Regulator Board) has reached +2.5V, as detected by comparator A9U2A.

7I-3. Over-Current Shutdown

Current-limiting is achieved by detecting the voltage drop across resistor A9R201. When excessive current flow is detected through A9R201 by comparator A9U2A, A9Q3 turns on hard and applies ground to the switching regulator's compensation pin 9. If the current through A9R201 exceeds approximately 14.7 Amps, pin 2 of A9U2A becomes more positive than pin 3, turning transistor A9Q3 on, and turning A9U1 off. When the –5.2V power supply output is shorted to ground, the current is limited to approximately 4.75 Amps. Both current limits are set by resistor chain A9R13, R15, R17, and R21.

Adjustable resistor A9R14 provides a fine adjustment for the –5.2V power supply.

7I-4. –3.3 Volt Linear Regulator

Voltage regulator A9U4 provides the +2.5 Vref for both error amplifier A9U3C and low-voltage detector A9U3A. Error amplifier A9U3C maintains, using feedback from the –3.3-volt output, the 1.9-volt difference across pass transistor A9Q5.

7I-5. Under-Voltage Shutdown

The low-voltage detector limits the –3.3V Power Supply output voltage to approximately –4.4 Volts by again using the compensation pin of A9U1 (pin 9) to shut off the –5.2V Switching Power Supply.

7I-6. Thermal Shutdown

To protect the HP 5371A from over heating, as would occur when the 120V circulating fan B1 fails, a heat-sensitive resistor A9R36 is mounted on the –3.3V supply's pass transistor A9Q5. If the case of transistor A9Q5 reaches approximately 128°F, A9Q9 shuts off, setting latch A12U7BD located on the Motherboard and shutting down the HP 5371A. Instrument power cannot be restored until the front-panel STBY-ON switch is cycled from ON-to-STBY-to ON.

7I-7. A10 TRIPLE REGULATOR BOARD

The schematic diagram for the A10 board is shown in *Figure 7I-2*.

The A10 Triple Regulator Board is comprised of three switching regulator circuits capable of producing +5-, +15- and –15-volt outputs.

7I-8. –15V Switching Power Supply

The –15V output is generated by switching regulator A10U6 which converts the +25V unregulated DC voltage into a regulated –15 Volts.

7I-9. –15V INPUT LC FILTER

The –15V regulator shares an LC input filter with the +15V regulator. This filter is comprised of A10 components L6, C5, C6, and C10. The unregulated +25 Vdc passes through inductor A10L6 to Pulse Width Modulator (PWM) A10U6 and to the pass transistor-diode network A10U2. The LC filter prevents the 40 kHz from entering the unregulated +25 Vdc source and consequently the AC power line source.

7I-10. –15V PULSE WIDTH MODULATOR

The PWM is an integrated circuit which contains a +5V reference, an error amplifier, an oscillator, a pulse width modulator, a pulse steering flip-flop, dual alternating output switches, and a shutdown circuit.

A10R51 and C26 set the internal oscillator frequency at 40 kHz nominal. A10U6, the –15V PWM, generates the 40 kHz ramp and 40 kHz oscillator pulses used by the PWM's in the +15V and +5V power supplies (A10U5 and U3 respectively). Therefore, if the for any reason the oscillator in A10U6 is inoperative, then the +12V and +5V power supplies will not operate.

The +5V reference from pin 16 of A10U6 is divided down to +2.5V by resistors A10R50 and R52 and is applied to the inverting input of the PWM's error amplifier. The –15V output voltage is sensed by A10 resistors R4, R7, and R8 and sent back to the non-inverting input of the PWM's error amplifier.

7I-11. –15V FREQUENCY COMPENSATION

A10C25 and R49, connected between pins 9 and 1 of PWM A10U6, provide frequency compensation and prevent oscillation in the feedback loop.

7I-12. –15V SOFT START CIRCUIT

Components R6, R24, CR5, and C8 provide "soft" start capability for the –15V power supply. As long as pin 9 of A10U6 is held low, the base drive to A10U2 is inhibited. When power is first applied to the circuit, capacitor A10C8 is discharged and pin 9 of A10U6 is held low by A10CR5. A10C8 begins to charge toward +25V which causes the voltage at pin 9 to ramp up. The base drive to A10U2 pin 3 will be 40 kHz pulses which increase in width until the voltage across A10C8 causes the voltage on pin 9 of A10U6 to rise to its steady state level.

The voltage across A10C8 continues to rise and reverse biases A10CR5. This causes the "soft" start circuitry to have no further effect upon the –15V PWM A10U6.

7I-13. –15V DARLINGTON (PASS) TRANSISTOR

This hybrid TO-3 packaged circuit contains a power Darlington and a fast-recovery, high-speed diode. The diode is connected in series with A10L9 and the –15V output. The Darlington is connected in series with A10L4, R27, and ground.

7I-14. –15V ENERGY STORAGE INDUCTOR

When the Darlington is turned on by the base drive generated by pins 12 and 13 of PWM A10U6 and applied through A10R28, current flows through A10L4 and R27 to ground. When the Darlington is turned off, the diode in A10U2 allows current to continue flowing through A10L4. This charges filter capacitor A10C17 which provides current to the load. A10R27 provides a voltage which is proportional to the current through A10L4. This voltage drives the current limiting circuitry.

7I-15. –15V CURRENT LIMITING CIRCUITRY

The voltage developed across A10R27 is applied through A10R30 to the base of transistor A10Q3. Under normal circumstances, A10Q3 is off. If the voltage across A10R27 exceeds +0.6V, A10Q3 turns on and discharges A10C8. This pulls pin 9 of A10U6 low, disabling A10U6 base drive output pins 12 and 13. This action turns the Darlington (pass) transistor in A10U2 off.

With the Darlington transistor off, the current through A10R27 goes to zero, A10Q3 turns off, and A10C8 begins to charge again. This causes pin 9 of A10U6 to go high, which enable the base driver pulse outputs. These pulses turn on the Darlington (pass) transistor. If the high-current condition still exists at the –15V output, A10Q3 again pulls pin 9 of A10U6 low causing the Darlington (pass) transistor to turn off. This process continues until the high-current condition across the –15V output is removed.

7I-16. –15V FILTER CAPACITOR

Filter capacitor, A10C17, smoothes out the 40 kHz ripple.

The output LC filter consisting of A10L9, C24, and C30 works with filter capacitor A10C17 to further reduce the 40 kHz ripple on the –15V output voltage.

7I-17. –15V DAMPING NETWORK

The damping network comprised of A10C7 and R29, is connected across filter capacitor A10C17 to provide gain and phase margin in the feedback loop. This circuit works by AC coupling a low value resistance, A10R29, across the LC circuit of A10L4 and C17.

7I-18. –15V VOLTAGE SENSE

The –15 Volts across filter capacitor A10C17 is sensed by the voltage divider of A10R4, R7, and R8. Part of the –15V output is fed back to pin 2 of PWM A10U6. This is the non-inverting input of the error amplifier.

7I-19. –15V SHUTDOWN

A TTL level signal can be applied to pin 10 of A10U6. This line is also connected to pin 10 of PWM A10U5 in the +15V power supply. A logic high is applied to the SHUTDOWN line to turn the A10 Triple Regulator Board off.

7I-20. +15V Switching Power Supply

The +15V Regulator is similar to the –15V Regulator. The main difference between the two is the manner in which the Darlington (pass) transistor and diode circuit of A10U1 are connected to provide a positive output instead of a negative output.

7I-21. +15V INPUT LC FILTER

A10 components L6, C5, C6, and C10 function as the input filter to the +15V Power Supply. This filter keeps RFI out of the AC input circuit, and prevents AC line transients from being applied to the +15V Power Supply.

7I-22. +15V ADJUSTMENT VOLTAGE DIVIDER

A10 resistors R3, R9, and R26 divide the +5-volt reference generated by PWM A10U5 down to +2.5 Volts. This reference voltage is applied to the non-inverting inputs of both the +5 Volt and the +15 Volt PWM error amplifier (A10U3 and A10U5 respectively).

7I-23. +15V PULSE WIDTH MODULATOR

The +15V Power Supply PWM is the same used in both the +5V and –15V supplies. The 40 kHz ramp and the 40 kHz oscillator pulses are generated by A10U6, the PWM in the –15V supply.

7I-24. +15V FREQUENCY COMPENSATION

A10C14 and R22 are connected between pins 9 and 1 of PWM A10U5 to provide frequency compensation of the feedback loop.

7I-25. +15V SOFT START CIRCUITRY

A10 components R47, C4, and CR7 provide "soft" starting for the +15V supply. A10CR10 provides a low impedance discharge path for capacitor A10C4 when the HP 5371A power is turned off. This ensures that the "soft" start function will function if the instrument's power cable is removed and reinstalled quickly with the front-panel STBY-ON switch in the ON position. A10CR2 prevents possible start-up problems by not allowing pin 9 of PWM A10U5 to go negative.

7I-26. +15V DARLINGTON (PASS) TRANSISTOR AND DIODE

A10U1 is the same hybrid used in the –15V Power Supply. However, the +15V supply's diode is connected to ground and the output of the Darlington (pass) transistor is connected to inductor A10L3. A10L3 stores the energy for the +15V supply. This arrangement provides a positive output voltage.

7I-27. +15V ENERGY STORAGE INDUCTOR

A10L3 is the energy storage element for the +15V Power Supply.

7I-28. +15V FILTER CAPACITOR

A10C16 filters the 40 kHz ripple from the +15-volt output.

7I-29. +15V OUTPUT LC FILTER

The output LC filter, consisting of A10 components L8, C23, and C29, works with filter capacitor A10C16 to further reduce the 40 kHz ripple on the output of the +15V Power Supply.

7I-30. +15V CURRENT LIMIT CIRCUITRY

The voltage across A10R38 is proportional to the +15-volt output current. This voltage is applied to comparator A10U4B. When the voltage exceeds 200 millivolts, the comparator switches and its output goes low (pin 2 of A10U4B). This allows capacitor A10C12 to discharge causing A10CR6 to pull pin 9 of PWM A10U5 low. This disables the gate drive output shutting off the Darlington (pass) transistor in A10U1. If the overload on the output remains, A10C4 will discharge through A10R37 allowing the +15V Power Supply to "soft" start when the overload condition has been removed.

7I-31. +15V VOLTAGE SENSE

The +15-volt output is divided down to +2.5 Volts by A10 resistors R46 and R48 and fed back to pin 1 of PWM A10U5. The feedback loop keeps the voltage at pin 1 equal to the reference voltage at pin 2.

7I-32. +15V OVERVOLTAGE PROTECTION

The overvoltage protection circuit consists of Zener diodes A10CR8 (17.8V) and CR9 (5.9V), resistors A10R43 and R44, and capacitor A10C21. If the +15V output rises to approximately 18.0 Volts, Zener diode A10CR8 begins to conduct, turning SCR A10CR14 turns on. This causes a large current to flow through the AC line fuse F1 blowing the fuse. The +25V unregulated supply must be removed to turn the SCR off.

A10 components R43, R44, and C21 provide noise immunity to the SCR gate.

7I-33. +15V SHUTDOWN

A TTL level signal can be applied to pin 10 of A10U5. This line is also connected to pin 10 of PWM A10U6 in the –15V power supply. A logic high is applied to the SHUTDOWN line to turn the A10 Triple Regulator Board off.

7I-34. +5 Volt Switching Power Supply

The +5V Power Supply is basically the same as the +15V supply except that the SHUTDOWN line is not connected to the +5V PWM A10U3.

7I-35. +5V INPUT LC FILTER

The input LC filter consists of A10L5, C1, and C20. As with the other two power supplies, this filter keeps 40 kHz interference out of the unregulated DC supply and AC input, and keeps AC line transients out of the +5-volt supply.

7I-36. +5V ADJUSTABLE VOLTAGE DIVIDER

The same resistive divider network used to set the +2.5-volt reference level for the +15V supply is used for the +5-volt supply.

7I-37. +5V PULSE WIDTH MODULATOR

The +5V PWM A10U3 is the same as those used in both the +15V and –15V supplies. The 40 kHz ramp and oscillator pulses are generated by the –15V PWM A10U6.

7I-38. +5V FREQUENCY COMPENSATION

Capacitor A10C18 and resistor A10R39 are connected between pins 9 and 1 of PWM A10U3 to provide frequency compensation of the feedback loop.

7I-39. +5V SOFT START CIRCUITRY

A10 components R53, C2, and CR11 provide "soft" starting for the +5 Volt supply. A10CR13 provides a low impedance discharge path for A10C2 when power is removed, allowing the "soft" start circuit to operate when power is reconnected.

7I-40. +5V DARLINGTON (PASS) TRANSISTOR AND DIODE

A10 transistors Q1 and Q2 make up the Darlington (pass) transistor and A10CR3 is the diode. The diode is connected to ground and the output of the pass transistor is connected to A10L2, which functions as the energy storage inductor. This arrangement provides a positive output voltage. A10Q4 provides drive current to A10Q2.

7I-41. +5V LC FILTER

The LC filter components A10L2 and C3 reduce the 40 kHz ripple in the +5 Volt output.

7I-42. +5V CURRENT LIMIT CIRCUITRY

The voltage drop across A10R45 is proportional to the current flowing out of the +5 Volt supply. This voltage is applied to comparator A10U4D. When the voltage exceeds 100 millivolts the comparator switches low (pin 13). This allows A10C19 to discharge and A10CR12 pulls pin 19 of PWM A10U3 low. This causes the Darlington (pass) transistor to turn off. If the overload on the output remains, A10R54 allows A10C2 to discharge. When the overload is removed, the +5 Volt regulator will "soft" start. This prevents the current limit circuitry from locking up when an overload occurs and then is removed.

7I-43. +5V OUTPUT LC FILTER

The output LC filter components A10L7, C22, and C28 further reduce the 40 kHz ripple on the +5 Volt output.

7I-44. +5V VOLTAGE SENSE

The +5 Volts at the A10R45-L2 junction is divided down to +2.5 Volts by A10 resistors R40 and R42 and fed back to pin one of the +5V PWM A10U3. The feedback loop keeps the voltage at pin 1 of A10U3 equal to the reference voltage at pin 2 of A10U3.

7I-45. +5V OVERVOLTAGE PROTECTION

If the +5 Volt output rises to +5.9 Volts, Zener diode A10CR9 begins to conduct. When the voltage rises to about +6.6 Volts, SCR A10CR14 turns on. This causes the AC line fuse F1 to blow, removing the DC input voltage to the regulator. A10 components R43, R44, and C21 provide noise rejection for the SCR's gate.

7I-46. A10 Inhibit Circuitry

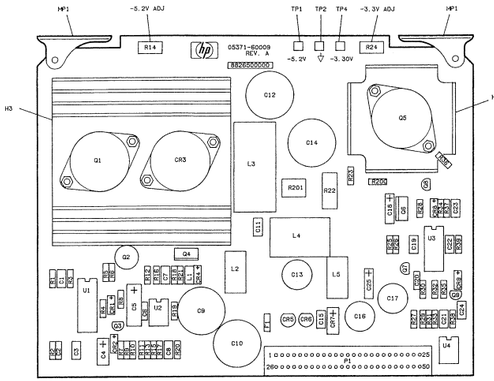
The +5 Volt and +15 Volt regulators are both inhibited from turning on until the –15 Volt supply is at least –10 Volts. The INHIBIT function is provided by components A10CR15, CR16, R55, and the internal current limiting circuitry to the +5 Volt and +15 volt PWMs (A10U3 and U5 respectively). When –15 Volt supply is less the -10 Volts, Zener diode A10CR16 conducts. This effectively grounds pin 4 of both A10U3 and U5.

7I-47. Power-up Reset

Comparators A10U4A and U4C are used as Schmitt triggers. The input of A10U4C, pin 9 of A10U4, is the output of the +5 Volt supply. When this output reaches +4.5 Volts, the A10U4C switches. RC network A10R14 and C11 provide a 120 millisecond delay before A10U4A switches. After the specified delay, the output of the second Schmitt trigger (pin 1 of A10U4) goes high, providing a POWER-UP RESET pulse for the A7 Processor Board's 68000 microprocessor. A10C13, located across the A10U4A input pins, prevents false triggering of the comparator due to 40 kHz noise.

7I-48. POWER SUPPLY TROUBLESHOOTING

Use the Schematic Diagrams, *Figures 7I-1* and *7I-2*, to troubleshoot the Power Supplies.



A9 SCHEMATIC DIAGRAM NOTES

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2. UNLESS OTHERWISE INDICATED:
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   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. R36 PHYSICALLY MOUNTED ON TRANSISTOR Q5.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

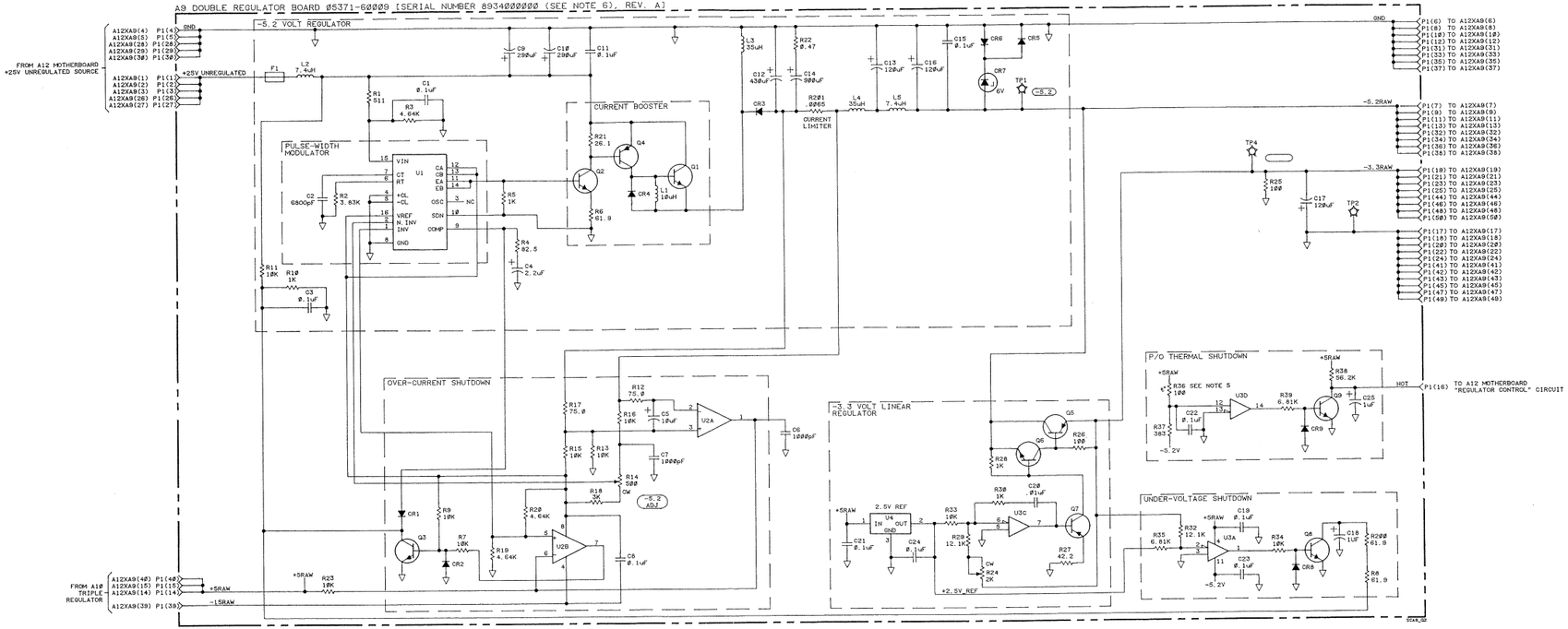
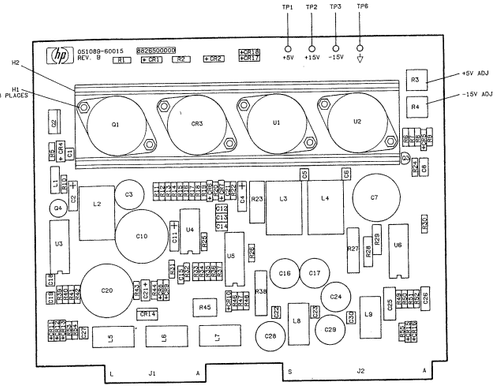


Figure 7I-1. A9 Double Regulator Board, Schematic Diagram



A10 SCHEMATIC DIAGRAM NOTES

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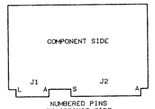
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. J1 AND J2 CONNECTOR CONTACT LABELING, COMPONENT SIDE: A-F, H, J-N, P, R-S.
6. J1 AND J2 CONNECTOR CONTACT LABELING, CIRCUIT SIDE: 1-15 OR 1-18.



7. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

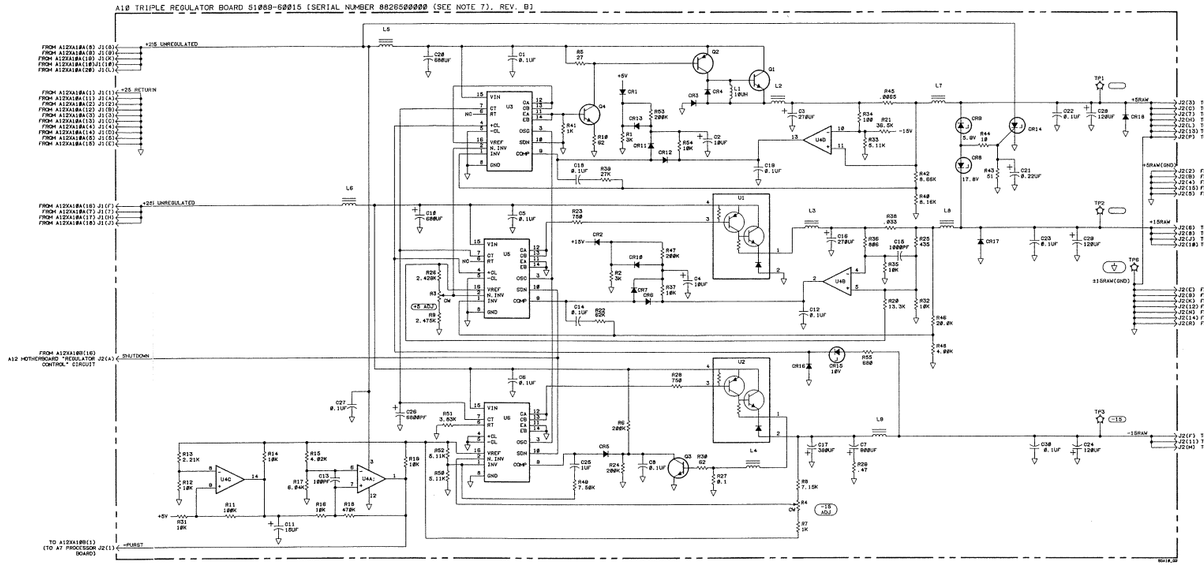


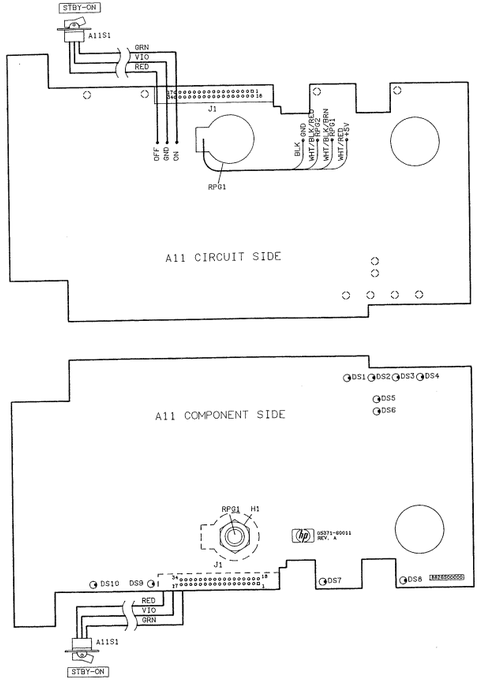
Figure 7I-2. A10 Triple Regulator Board, Schematic Diagram

7J A11 FRONT PANEL BOARD

SECTION 7J
A11 FRONT PANEL BOARD

Front Panel Board A11 contains LED's and switches for the HP 5371A front panel. *Figure 7J-1* shows the schematic diagram for A11. Note that the ENTRY/MARKER control and the STBY-ON switch are supplied with the Front Panel Board.

A11 interconnects the various components to I/O Controller Board A8.



A11 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A11 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THE FRONT PANEL ENTRY/MARKER KNOB, OR ROTARY PULSE GENERATOR (RPG1), AND FRONT PANEL STBY-ON SWITCH ARE SUPPLIED WITH THE 05371-60011 BOARD.
6. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

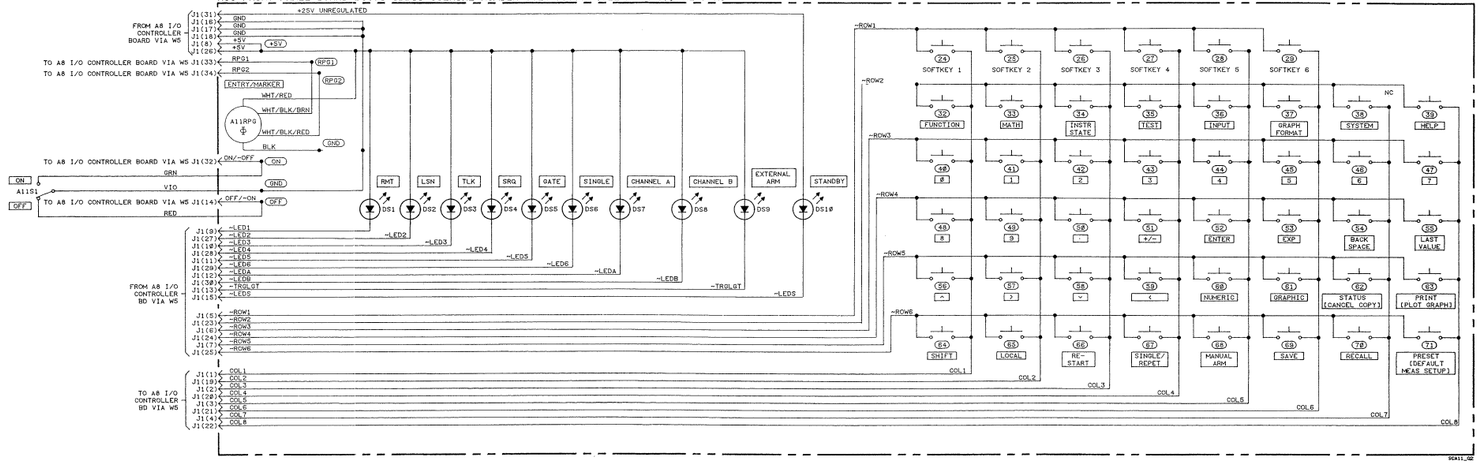


Figure 7-1. A11 Front Panel Board, Schematic Diagram

SECTION 7K
A12 MOTHERBOARD

7K-1. OVERVIEW

The A12 Motherboard provides power distribution, power-up control, rear-panel signal buffering, communication paths between the different assemblies (i.e., A1, A2, A4, A5 . . . etc.), power regulation for the internal reference oscillator's oven and crystal, fan control, power failure monitoring circuitry, and thermal overload control.

The communication paths are provided in the form of busses that allow the boards installed to interact. The busses consist of data lines, address lines, and several control lines. The A12 Motherboard provides power and signal flow paths (busses) for all printed circuit boards installed in the HP 5371A card cage. The major signals are the system data lines, measurement data lines, address lines, HP-IB lines, miscellaneous control lines, and all power distribution lines. The digital signals are divided into two different busses, the System Bus and the Count Hardware bus, to isolate the digital noise from the counting hardware. Data, address, and control lines from one bus to the other is latched through buffers located on the A7 Processor Board. The Count hardware bus can be turned off when not in use.

The schematic diagram for A12 is shown in *Figure 7K-1* at the back of this section.

The OFF signal has two states, depending on the front-panel ON-STBY switch (S1). When in the ON position, the OFF signal is grounded. On the A12 assembly, the OFF signal influences the Off Delay, Fan Control, and Power Fail Interrupt circuitry.

When the front-panel ON-STBY switch is placed in the STBY position, the OFF signal line goes high (+25 Volts nominal unregulated, but can reach voltages up to +35 Volts nominal) and grounds the cathode side of the front-panel STANDBY LED (A11DS10). This lights the STANDBY LED. By placing the instrument in standby, you effectively remove all power except the power applied (signal LP) to back-up RAMs A7U50 and A7U51 located on the A7 Processor Board and the A15 oscillator's internal oven. The "Power Fail Interrupt Control" circuit generates an interrupt signal called ~POWERFAIL that informs the A7 assembly's 68000 microprocessor that power has been removed. Upon switching the front-panel ON-STBY switch to ON, the microprocessor resets this circuit via the ~RESET signal.

7K-2. Power-Fail Interrupt Control

During a temporary power loss, such as could occur when the ON-STBY switch is turned ON-to-STBY-to-ON rapidly, the "Power Fail Interrupt Control" circuit generates and latches an interrupt signal (~POWERFAIL) and sends it to the microprocessor. The microprocessor goes through an internal power-down subroutine, senses that the power interruption was a temporary one, and initiates a power-up sequence, then resets the A12U10B and U10D flip-flop via the ~RESET signal.

7K-3. Off Delay

When the front-panel switch is set to STBY position, node A12R28-R29 is pulled from 0 to approximately +25 Volts. Capacitors A12C11 and C12 begin to charge. When the voltage at op-amp U6C pin 9 exceeds approximately +12 Volts, A12U6C generates a pulse and sends it to the "Regulator Control" circuit. The pulse is latched by gates A12U7A, U7B, and U7D. The resulting output signal, SHUTDOWN, is routed to the A10 Triple Regulator Board, where it shuts down the +5V, +15V, and -15V switching power supplies. The +5V and -15V supplies, in turn, shut down the -5.2 and -3.3 Volt output voltages of the A9 Double Regulator Board.

7K-4. Power-Fail Detect

Power-Fail Interrupt Control is also driven by the "Power-Fail Detect" circuit. The "Power-Fail Detect" circuit monitors the unfiltered AC voltage, AC1 and AC2, from the secondary of center-tapped power transformer T1. Diodes A12CR2 and CR3 locally rectify AC1 and AC2. If the rectified voltage drops below a set threshold of approximately +12.5 Volts, op-amp A12U6D generates a pulse and sends it to the "Power-Fail Interrupt Control" circuit. This circuit responds by generating an interrupt and sending it on to the A7 Processor Board's 68000 microprocessor. The interrupt is generated fast enough so that the microprocessor can execute its power-down sequence prior to chassis-mounted, filter capacitor C1 (+25V unregulated) having a chance to discharge.

7K-5. Regulator Control Block

The Regulator Control Block circuitry determines whether the A10 Triple Regulator or the A9 Dual Regulator assembly are generating output voltages or not.

The HOT signal, which terminates in the A12 "Regulator Control" circuit (A12U7C pin 10), originates from excessive heat generated by pass transistor A9Q5 of the -3.3V power supply of the A9 Double Regulator Board. A thermal overload condition causes the HOT signal to set and latch the "Regulator Control" flip-flop. This circuit shuts down the A10 Triple Regulator and then the A9 Double Regulator assemblies. The front-panel ON-STBY switch is set to ON, the STBY LED is off, but the fan remains on. The instrument remains off even after the instrument cools off. To turn the A10 and A9 regulators on after cool-down, the front-panel STBY-ON switch must be turned from ON-to-STBY-to ON. This process resets the "Regulator Control" circuit. This circuit requires user intervention following a thermal overload.

7K-6. Power-on Reset

This circuit ensures that the Regulator Control circuit is in the proper state following application of power to the HP 5371A. When the +5P power source reaches the required threshold, the circuit output sets the "Regulator Control" circuit.

7K-7. +5P Power Supply

This "permanent" +5 Volt supply is used for the A12 Motherboard circuitry only. Regulator A12U3 drops +25V unregulated to a regulated +5 Volts (+5P).

7K-8. LP Power Supply

"LP" is the low power applied to the A7 back-up A7 RAMs A7U50 and A7U51 when the front-panel ON-STBY switch is set to STBY. This supply saves battery A7BT1, mounted on the A7 Processor Board, for use when the HP 5371A is disconnected from AC power or when the A7 assembly is physically removed from the instrument's chassis. The local rectifier, A12CR2 and A12CR3, is the point of origin for the LP voltage.

7K-9. +21V Oven Power Supply

The +21V Oven Regulator U11 regulates the +25V unregulated voltage down to approximately +21 Volts. +21 Volts is the voltage required to operate the internal oven of the A15 Oven Oscillator. This power supply is on as long as the HP 5371A is connected to AC power.

7K-10. +12OSC Power Supply

When a rear-panel "External Input" frequency standard is not detected by the A1 Timebase Control assembly, the +15OSC line is enabled. This in turn provides the input voltage to regulator A12U8 on the A12 assembly. Regulator A12U8 output, +12OSC, supplies power to the internal 10 MHz A15 Oven Oscillator assembly.

7K-11. +12CRT Power Supply

This power supply provides the CRT Driver Board with +12 Volts. +15 Volts from the A10 assembly is regulated down to +12 Volts by regulator A12U2.

7K-12. Overvoltage Transorber

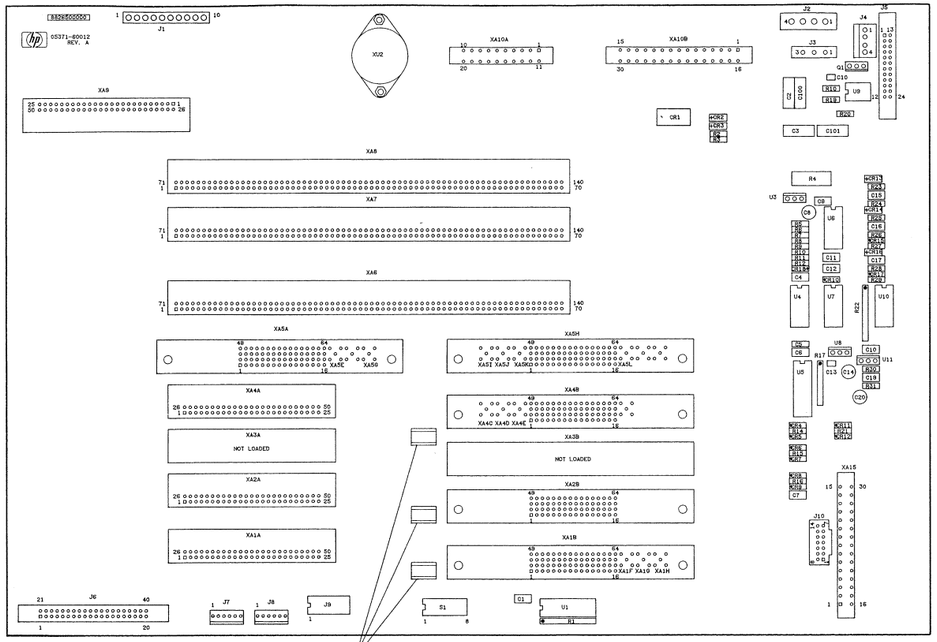
A12CR1, mounted on the A12 Motherboard, prevents the +5 Volts derived on the A10 Triple Regulator Board from rising to levels that could damage the components using this power source. A12CR1 clamps the +5-volt line to approximately 6 Volts. The extra current flow through CR1 will cause the line fuse F1 to open.

7K-13. Option Switch Circuit

Option Switch A12S1 is preset at the factory to correspond to any options provided with the HP 5371A. Currently, only two settings are possible: all switches closed (in their left-most position) for a standard unit (with no options), and switch 2 (second from front of instrument) closed for Option 060 (Rear-panel inputs). A12S1 determines the bit configuration read by A7 microprocessor via Count Hardware Data Bus (CTD0-CTD6) when the HP 5371A is first powered on. Line driver A12U1 places the bit configuration on the Count Hardware Bus when signal CTCS7 (from demultiplexer A7U43) switches low. Signal ~CHDTK is also simultaneously sent to PAL IC A1U21, where it is decoded and controls the reading of POD I.D. information by the A7 68000 microprocessor.

7K-14. Rear Panel Output Buffers

The Rear Panel Output Buffers, A12U5ABCD, provide signals [falling-edge active, TTL levels into >=10K(OHM) or 0V-to-1V (minimum) into 50(OHM)] to the instrument's rear panel OUTPUTS BNC connectors via coaxial W3 and the A13 Rear Panel Board. GATE 1 (Start) and GATE 2 (Stop) outputs are buffered by A12U5BC and provide an indication of when measurement samples occur. Both signals are essentially buffered versions of the IT1 (Start) and IT2 (Stop) interpolator trigger signals generated by the A5 ZDT/Count Board. The ARM 1 DELAY and ARM 2 DELAY outputs are buffered by A12U5AF and indicate when time or event conditions have been satisfied. The ARM DELAY signals are buffered versions of the TC1/P1 and TC/P2 signals generated by the A5 ZDT counter ICs.



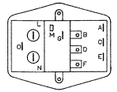
A12 SCHEMATIC DIAGRAM NOTES

NOTES

1. REFERENCE DESIGNATIONS WITHIN EACH ASSEMBLY ARE ABBREVIATED. ADD A8,A11 OR A12 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. LINE FUSE F1.

LINE VOLTAGE (NOMINAL)	FUSE		LINE VOLTAGE SELECTION SWITCH POSITIONS	
	RATING	HP PART NUMBER	CLOSED	OPENED
100 ± 10%	4A NO TIME DELAY	2110-0055	a, c, e	b, d
120 ± 10%			b, c, e	a, d
220 ± 10%	2A NO TIME DELAY	2110-0002	a, d	b, c, e
240 ± 10%			b, d	a, c, e

6. SEE SECTION VI FOR PROCEDURES TO REPLACE FUSE F1 OR TO CHANGE THE LINE VOLTAGE SELECTOR SETTING.
7. THE ILLUSTRATION BELOW IS A REAR VIEW PINOUT OF A16 POWER MODULE ASSEMBLY AS VIEWED FROM INSIDE THE INSTRUMENT.



8. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

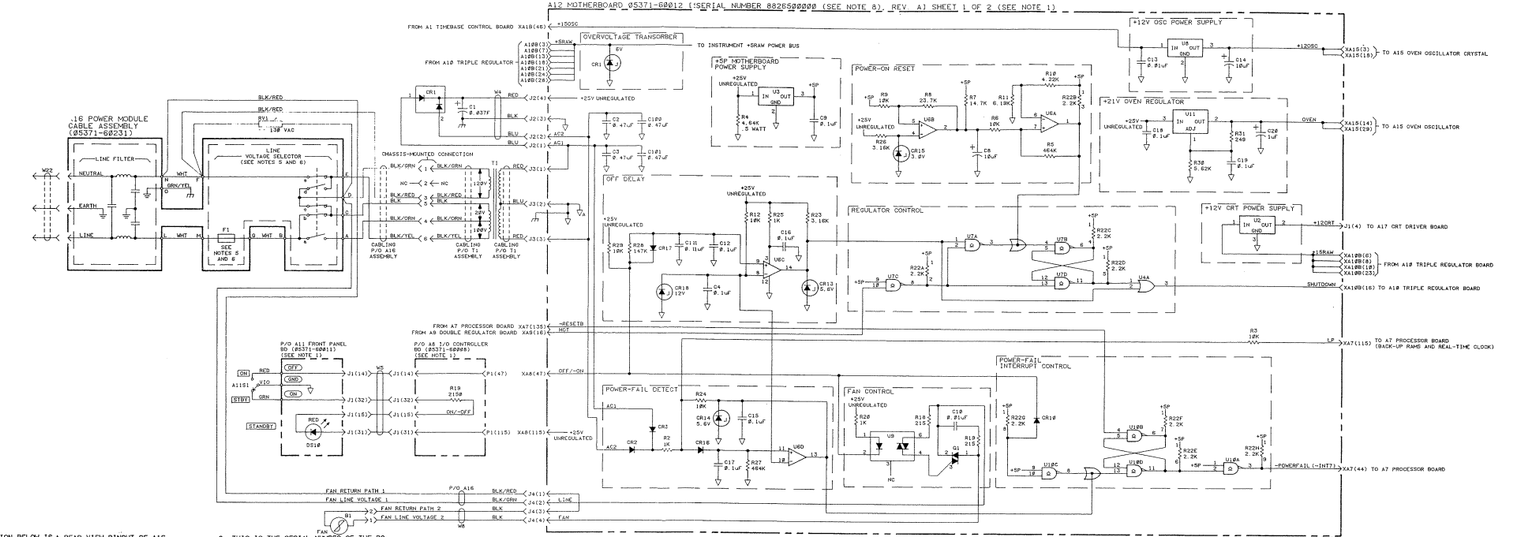
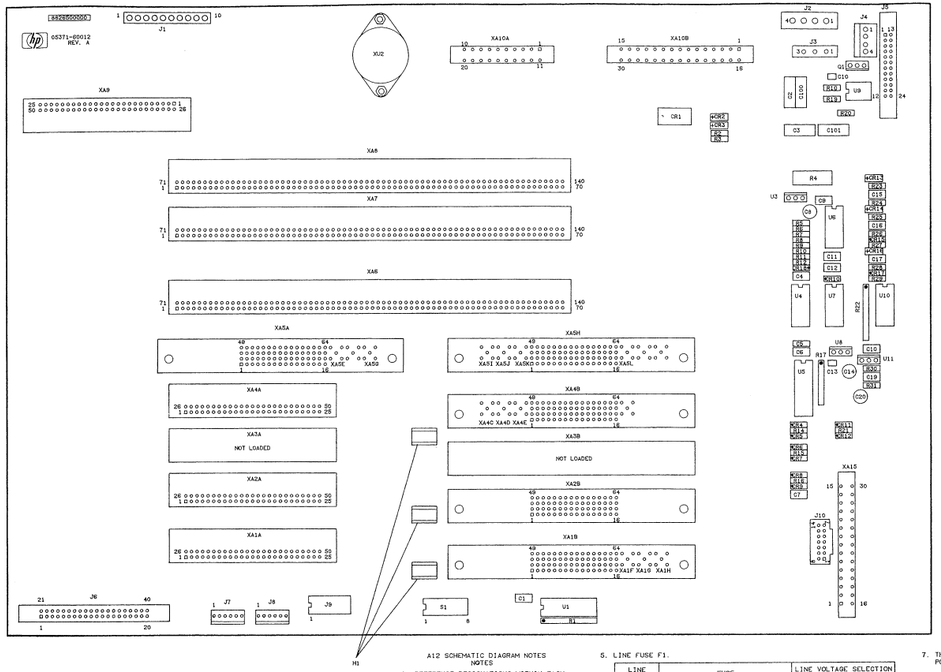


Figure 7K-1. A12 Motherboard, Schematic Diagram
(Sheet 1 of 2)



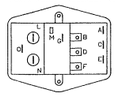
A12 SCHEMATIC DIAGRAM NOTES

NOTES

1. REFERENCE DESIGNATIONS WITHIN EACH ASSEMBLY ARE ABBREVIATED. ADD A8,A11 OR A12 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. LINE FUSE F1.

LINE VOLTAGE (NOMINAL)	FUSE		LINE VOLTAGE SELECTION SWITCH POSITIONS	
	RATING	HP PART NUMBER	CLOSED	OPENED
100 ± 10%	4A NO TIME DELAY	2110-0055	a, c, e	b, d
120 ± 10%			b, c, e	a, d
220 ± 10%	2A NO TIME DELAY	2110-0002	a, d	b, c, e
240 ± 10%			b, d	a, c, e

6. SEE SECTION VI FOR PROCEDURES TO REPLACE FUSE F1 OR TO CHANGE THE LINE VOLTAGE SELECTOR SETTING.
7. THE ILLUSTRATION BELOW IS A REAR VIEW PINOUT OF A16 POWER MODULE ASSEMBLY AS VIEWED FROM INSIDE THE INSTRUMENT.



8. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

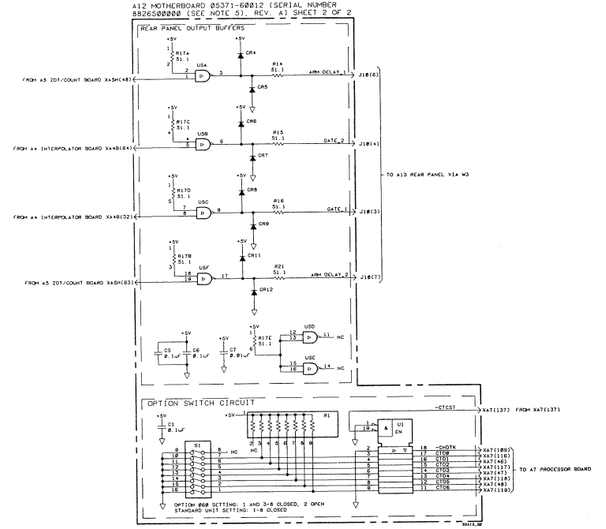
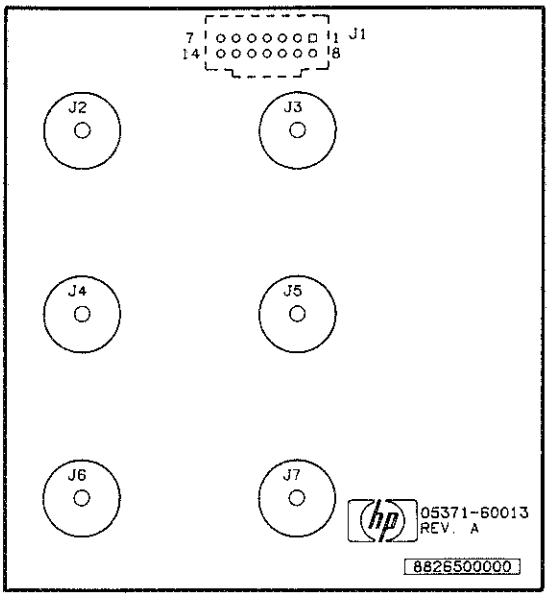


Figure 7K-1. A12 Motherboard, Schematic Diagram (Sheet 2 of 2)

7L A13 REAR PANEL BOARD

SECTION 7L
A13 REAR PANEL BOARD

The Rear Panel Board A13 serves to interconnect signals from Motherboard A12 to connectors on the rear panel. The schematic diagram is shown in *Figure 7L-1.*



A13 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A13 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. THIS IS THE SERIAL NUMBER OF THE PC BOARD. ENGINEERING CHANGES ARE KEYED TO THE 5-DIGIT PREFIX OF THE SERIAL NUMBER. TO TRACK ENGINEERING CHANGES THAT MAY HAVE OCCURRED SINCE MANUAL'S LAST PRINTING, REFER TO YELLOW "MANUAL UPDATING CHANGES" SHEETS. FOR MORE DETAILS, SEE "IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS" PARAGRAPH IN SECTION 7.

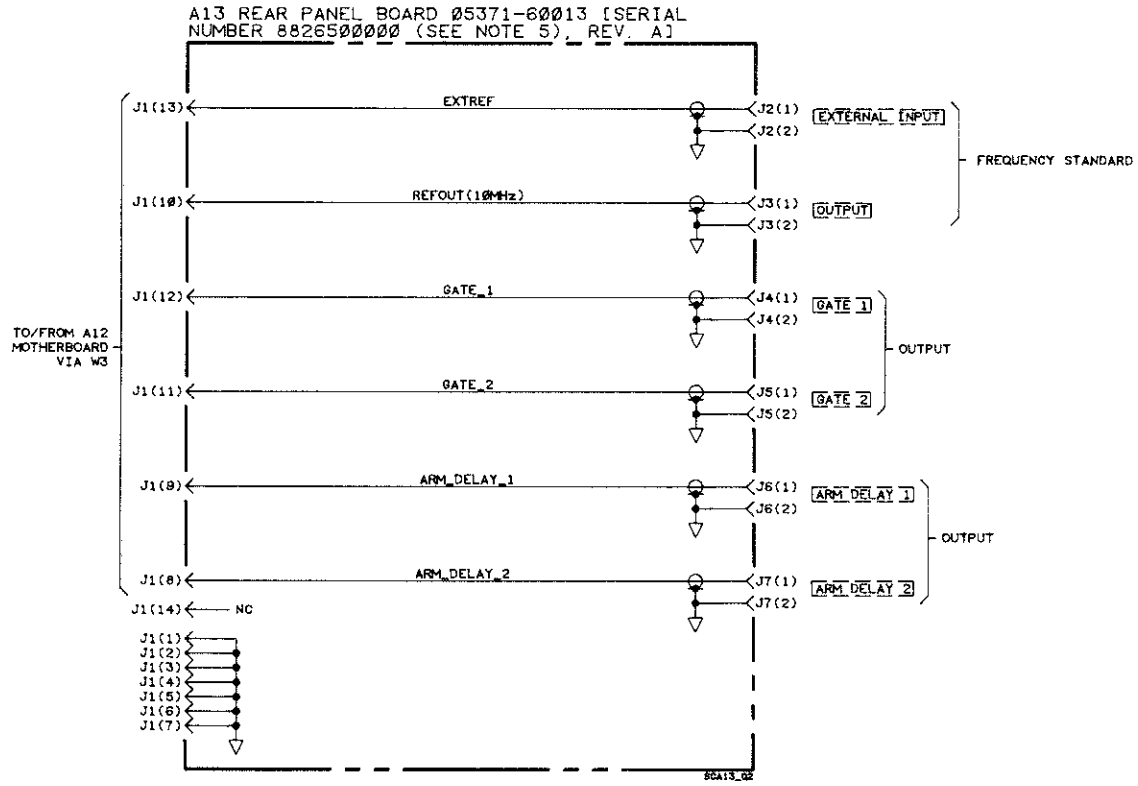


Figure 7L-1. A13 Rear Panel Board, Schematic Diagram

7M A15 OVEN OSCILLATOR

SECTION 7M
A15 OVEN OSCILLATOR ASSEMBLY

This section has been deleted. See the separate manual for the HP 10811A/B Quartz Crystal Oscillator, Manual Part Number 10811-90002.

7N ASSEMBLY AND CABLE LOCATIONS

SECTION 7N
ASSEMBLY AND CABLE LOCATIONS

ASSEMBLY IDENTIFICATION AND LOCATION

The assembly number, name, and Hewlett-Packard part number of the 5371A assemblies are listed in *Table 7N-1*. A top internal view is shown in *Figure 7N-1*.

Table 7N-1. HP 5371A Assembly Identification

Assembly	Name	HP Part Number
A1	Timebase Control Board	05371-60001
A2	Input Amplifier Board	05371-60002
A3	NOT ASSIGNED	
A4	Interpolator Board	05371-60004
A5	ZDT/Count Board	05371-60027
A6	DMA/Gate Board	05371-60018
A7	Processor Board	05371-60007
A8	I/O Controller Board	05371-60008
A9	Double Regulator Board	05371-60009
A10	Triple Regulator Board	51089-60015
A11	Front Panel Board	05371-60011
A12	Motherboard	05371-60012
A13	Rear Panel Board	05371-60013
A14	Timebase Multiplier Board	05371-60014
A15	Oven Oscillator Assembly	10811-60111
A16	Power Module Cable Assembly	51083-60108
A17	CRT and Driver Board	2090-0209

CABLES

Table 7N-2 lists all cables used in the HP 5371A. They are listed in numerical order (reference designator) followed by HP Part Number, description, source and destination information. *Figure 7N-1* is a top view of the 5371A showing the cabling layout.

Table 7N-2. HP 5371A Cabling

Reference Designator	HP Part Number	Description	Cable Connection Description
A5W1	05371-60218	The Count Cable Assembly is a coaxial cable (right-angle SMC to coaxial termination) that routes the conditioned EECL-level input signal, OUTPUT_CH_A, from the A2 Input Amplifier Board to the A5 ZDT/Count Board. A5W1 is part of the A5 assembly.	From A2J2 to A5W1
A5W2	05371-60218	The Count Cable Assembly is a coaxial cable (right-angle SMC to coaxial termination) that routes conditioned EECL-level input signal, OUTPUT_CH_B, from the A2 Input Amplifier Board to the A5 ZDT/Count Board. A5W2 is part of the A5 assembly.	From A2J4 to A5W2
W1		NOT ASSIGNED	
W2		NOT ASSIGNED	
W3	8120-4965	The 50Ω Ribbon Cable Assembly is a ribbon cable that transfers the rear-panel input signal (1, 2, 5, 10 MHz EXTERNAL INPUT) and the output signals (10 MHz OUTPUT, ARM DELAY 1 & 2, and GATE 1 & 2 OUTPUTS) between the A13 Rear Panel Board and A12 Motherboard.	A13J1 to/from A12J10
W4	05371-60201	The Power Supply Cable Assembly routes secondary ac voltage AC1 and AC2 to the chassis-mounted rectifier (CR1) and returns +25V dc (unregulated), via the chassis-mounted filter capacitor (C1), to the A12 Motherboard.	A12J2 to/from chassis-mounted components CR1 and C1.

Table 7N-2. HP 5371A Cabling (Continued)

Reference Designator	HP Part Number	Description	Cable Connection Description
W5	05371-60202	The Front Panel Cable Assembly is a 34-conductor ribbon cable that routes (1) all 5371A data entered via the front-panel keypad or ENTRY/MARKER Knob (RPG), (2) all front-panel LED control signals and LED power supply voltages [+25V dc (unregulated) to red "STANDBY" LED and +5V dc to all other LEDs], and (3) front-panel STBY-ON power switch (S1) control lines to/from the A8 I/O Controller Board.	A8J1 to/from A11J1
W6	05371-60204	The DMA Cable Assembly is a 50-conductor ribbon cable that routes thirteen Measurement RAM address lines from the A6 DMA/Gate Board to the A5 ZDT/Count Board. W6 also routes miscellaneous control lines between the A5 and A6 assemblies.	A5J2 to/from A6J1.
W7	05371-60205	The HP-IB Cable Assembly is a 24-pin HP-IB that transfers the bidirectional HP-IB bus (data, handshake and control lines) from the A8 I/O Controller Board (via the A12 Motherboard) to the 5371A rear-panel HP-IB connector.	A12J5 to/from 5371A rear-panel 24-conductor cable connector.
W8	05371-60206	The Fan Cable Assembly is a 2-conductor that routes a 120V ac line and a return (neutral) line from the A12 Motherboard to the B1 Cooling Fan.	A12J4 to/from B1 Cooling Fan.
W9	05371-60207	The External Arming Cable Assembly is a coaxial cable (BNC to SMB) that routes the 5371A front-panel EXTERNAL ARM input to the front bulkhead where it connects with cable W21. W21 routes the signal from the front bulkhead to A6J1 of the A6 DMA/gate Board.	From front-panel "EXTERNAL ARM" input to the front bulkhead.

Table 7N-2. HP 5371A Cabling (Continued)

Reference Designator	HP Part Number	Description	Cable Connection Description
W10	05371-60208	The Channel A Rear Panel Input Cable Assembly is a coaxial cable (BNC to SMA) that routes the OPTION 060 CHANNEL A rear-panel input to the front bulkhead where it connects with cable W19. W19 routes the signal from the front bulkhead (top hole) to A2J1 of A2 Input Amplifier Board. *Available with Option 060 ONLY.*	From rear-panel "OPTION 060 CHANNEL A" input to the front bulkhead (top hole).
W11	05371-60208	The Rear Panel Channel B Input Cable Assembly is a coaxial cable (BNC to SMA) that routes the OPTION 060 CHANNEL B rear-panel input to the front bulkhead where it connects with cable W20. W20 routes the signal from the front bulkhead (bottom hole) to A2J3 of the A2 Input Amplifier Board. *Available with Option 060 ONLY.*	From rear-panel "OPTION 060 CHANNEL B" input to the front bulkhead (bottom hole).
W12	05371-60215	The Rear Panel External Arm Input Cable Assembly is a coaxial cable (BNC to SMC) that routes OPTION 060 EXTERNAL ARM rear-panel input to the front bulkhead where it connects with cable W21. W21 routes the signal from the bulkhead to A6J1 of the A6 DMA/Gate Board. *Available with Option 060 ONLY.*	From rear-panel "OPTION 060 EXTERNAL ARM" input to the front bulkhead.
W13	05371-60216	The 1 MHz Clock Cable Assembly is a coaxial cable (right-angle to right-angle SMB) that routes the 1 MHz reference frequency from the A1 Timebase Control Board to the Phase-Locked Loop (PLL) circuit located on the A14 Timebase Multiplier Board.	From A1J1 to A14J7.

Table 7N-2. HP 5371A Cabling (Continued)

Reference Designator	HP Part Number	Description	Cable Connection Description
W14	05371-60216	The 10MHz (ECL) Clock Cable Assembly is a coaxial cable (right-angle to right-angle SMB) that routes a 10 MHz frequency from the A14 Timebase Multiplier Board to the A1 Timebase Control Board where it is buffered and sent (via the A12 Motherboard) to the rear-panel 10 MHz FREQUENCY STANDARD OUTPUT.	From A14J5 to A1J2.
W15	05371-60217	The DMA Clock Cable Assembly is a coaxial cable (right-angle SMC to right-angle SMC) that routes the 125 MHz ECL-level DMACLK signal from the A14 Timebase Multiplier Board to the A5 ZDT/Count Board.	From A14J8 to A5J1.
W16	05371-60220	The 500 MHz Clock Cable Assembly is a coaxial cable (right-angle SMC to right-angle SMC) that routes a 500 MHz reference frequency (CLKA) from the A14 Timebase Multiplier Board to the A4 Interpolator Board.	From A14J9 to A4J2.
W17	05371-60220	The 500 MHz Clock Cable Assembly is a coaxial cable (right-angle SMC to right-angle SMC) that routes a 500 MHz reference frequency (CLKB) from the A14 Timebase Multiplier Board to the A5 ZDT/Count Board.	From A14J10 to A5J3.
W18	05371-60221	The Timebase Power Supply Cable Assembly is a 4-conductor cable that routes +10V dc, –10 V dc, –5.2V dc, and the Phase-Locked Loop's (PLL) control voltage (VT500) between the A14 Timebase Multiplier Board and the A1 Timebase Control Board.	Supply voltages are routed from A1J3 to A14J2, J3, and J4. The PLL control voltage is routed from A14J1 to A1J1.

Table 7N-2. HP 5371A Cabling (Continued)

Reference Designator	HP Part Number	Description	Cable Connection Description
W19	05371-60222	The Pod Cable Assembly is a coaxial cable (SMA bulkhead to right-angle SMA) that routes the CHANNEL A input signal from either the front-panel input pod or the rear-panel Option 060 CHANNEL A input to the A2 Input Amplifier Board.	From the front bulkhead (top hole) to A2J1.
W20	05371-60222	The Pod Cable Assembly is a coaxial cable (SMA bulkhead to right-angle SMA) that routes the CHANNEL B input signal from either the front-panel input pod or the rear-panel Option 060 input A2 Input Amplifier Board.	From front bulkhead (bottom hole) to A2J3.
W21	05371-60223	The External Arming Extension Cable Assembly is a coaxial cable (right angle to right-angle SMB) that routes either the EXTERNAL ARM input signal from either the front-panel input or the rear-panel Option 060 input to the A6 DMA/Gate Board.	From front bulkhead to A6J2.
W22	8120-1378	The Power Cable Assembly is a 3-conductor power cable used to connect the 5371A 120/220 ac power.	Connects A16 Power Module Cable Assembly to an external ac source.
W23	54100-67602	The Pod Power/Pod Identification Cable Assembly is comprised of two cable subassemblies. A 6-conductor cable transfers the CHANNEL A 3-bit Input Pod ID code and the ± 10V dc Pod Power to/from the A1 Timebase Control Board (via the A12 Motherboard). A coaxial cable routes the CHANNEL A input signal to the front bulkhead (top hole) where it connects with cable W19. W19 routes the input signal to the A2 Input Amplifier Board.	The CHANNEL A Input Pod's 6-conductor cable connects to the A12 Motherboard at A12J7. The coaxial cable is connected to W19 at the front bulkhead (top hole).

Table 7N-2. HP 5371A Cabling (Continued)

Reference Designator	HP Part Number	Description	Cable Connection Description
W24	54100-67602	The Pod Power/Pod Identification Cable Assembly is comprised of two cable subassemblies. A 6-conductor cable transfers the CHANNEL A 3-bit Input Pod ID code and the ±10V dc Pod Power to/from the A1 Timebase Control Board (via the A12 Motherboard). A coaxial cable routes the CHANNEL B input signal to the front bulkhead (top hole) where it connects with cable W20. W20 routes the input signal to the A2 Input Amplifier Board.	The CHANNEL A Input Pod's 6-conductor cable connects to the A12 Motherboard at A12J8. The coaxial cable is connected to W20 at the front bulkhead (bottom hole).

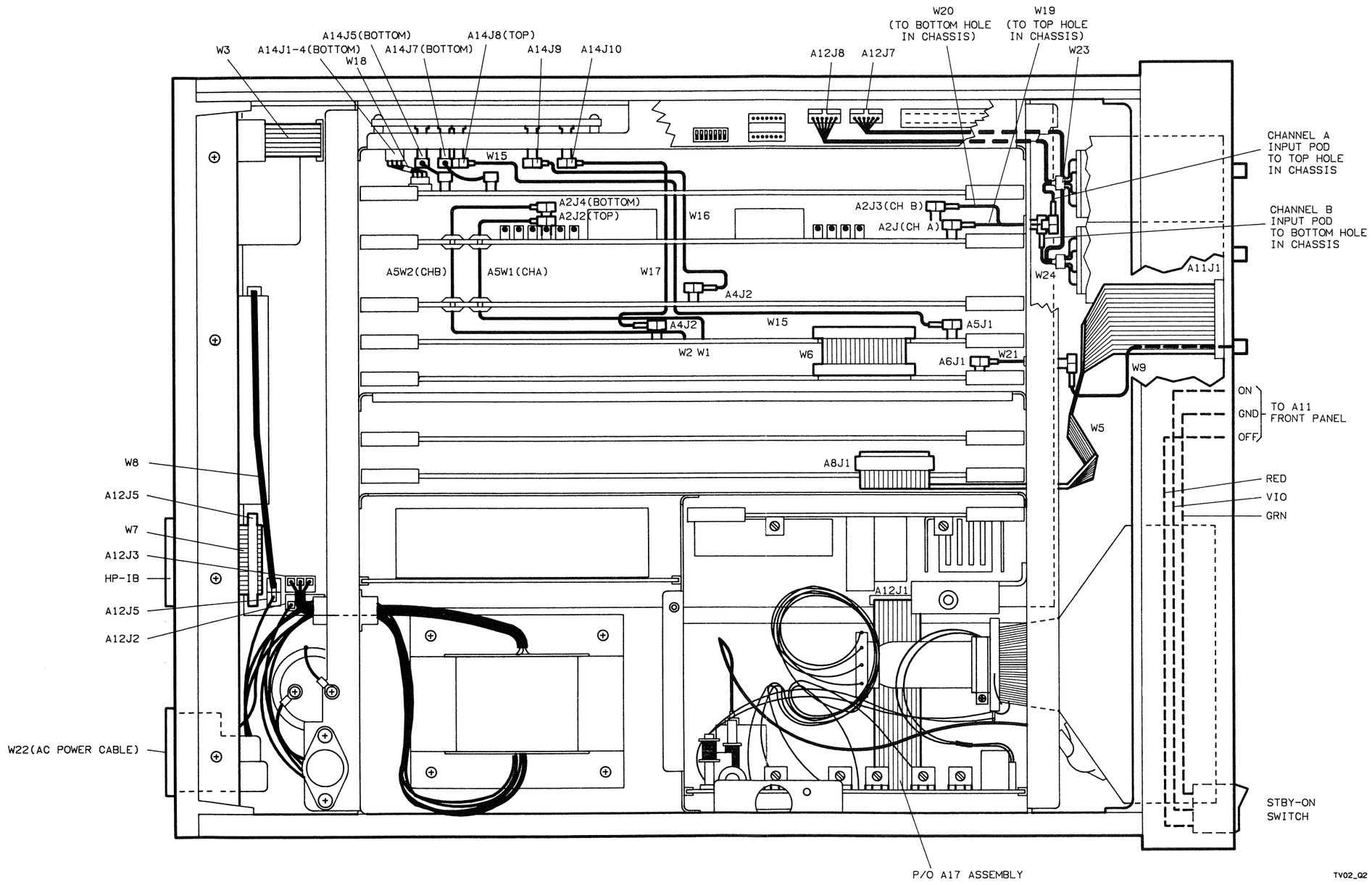


Figure 7N-1. HP 5371A Top Internal View

SECTION 7O
DISASSEMBLY AND REASSEMBLY

7O-1. DISASSEMBLY AND ASSEMBLY

NOTE

Throughout this section, references will be made to MP numbers and to various items of nomenclature. Use *Figure 7O-2* to identify the various items of hardware. *Figure 7O-2* is the foldout diagram located at the back of this section and contains the Illustrated Parts Breakdown (IPB) for the HP 5371A.

Prior to performing disassembly and reassembly procedures, the following steps must be performed:

a. Set front-panel power STBY-ON switch to STBY position.

b. Remove AC line power cable from rear-panel power module to disconnect the HP 5371A from the power mains.

WARNING

WHEN THE COVERS ARE REMOVED FROM THE HP 5371A, LINE VOLTAGES ARE EXPOSED WHICH ARE DANGEROUS AND MAY CAUSE SERIOUS INJURY IF TOUCHED. TO PREVENT ELECTRIC SHOCK, BE SURE THE INSTRUMENT FRONT-PANEL STBY-ON SWITCH IS SET TO THE STBY POSITION AND THE AC POWER CABLE IS REMOVED BEFORE PERFORMING ANY OF THE DISASSEMBLY PROCEDURES IN THIS SECTION.

CAUTION

IN THE FOLLOWING STEPS, BE CAREFUL TO AVOID DAMAGE TO ATTACHED COAXIAL AND FLAT-RIBBON CABLES. DISCONNECT COAXIAL CABLES FROM PC BOARDS PRIOR TO COMPLETE REMOVAL OF ASSEMBLY.

CAUTION

THE ELECTRICAL ASSEMBLIES AND COMPONENTS INVOLVED IN THE FOLLOWING STEPS ARE ALL STATIC SENSITIVE. TO PREVENT ELECTROSTATIC DAMAGE, ALL ASSEMBLIES AND COMPONENTS SHOULD BE HANDLED AT A STATIC-FREE WORK STATION, AND IN ACCORDANCE WITH THE PROCEDURES DESCRIBED IN THE ELECTROSTATIC DISCHARGE PARAGRAPHS.

The following tools are required for these procedures:

a. Large (2 point) Pozidriv screwdriver

b. Small (1 point) Pozidriv screwdriver

c. Needle-nose pliers

d. 6 mm open-end wrench

e. 8 mm open-end wrench

This section provides removal and installation procedures for the key 5371A assemblies listed below. Installation procedures for field installation of Option 060 is also provided.

- Input Pod (HP 54001A, HP 54002A, or HP 54003A)
- 5371A Top Cover
- 5371A Bottom Cover
- 5371A Side Cover
- Front-panel Assembly
- A1 Timebase Control Board
- A2 Input Amplifier Board
- A4 Interpolator Board
- A5 ZDT/Count Board
- A6 DMA/Gate Board
- A7 Processor Board
- A8 I/O Controller Board
- A9 Double Regulator Board
- A10 Triple Regulator Board
- A11 Front Panel Board
- A12 Motherboard
- A13 Rear Panel Board
- A14 Timebase Multiplier Board
- A15 Oven Oscillator Assembly
- A17 CRT and Driver Board
- B1 Cooling Fan

Figure 7O-1 shows the HP 5371A Top Internal View and the locations of the various assemblies.

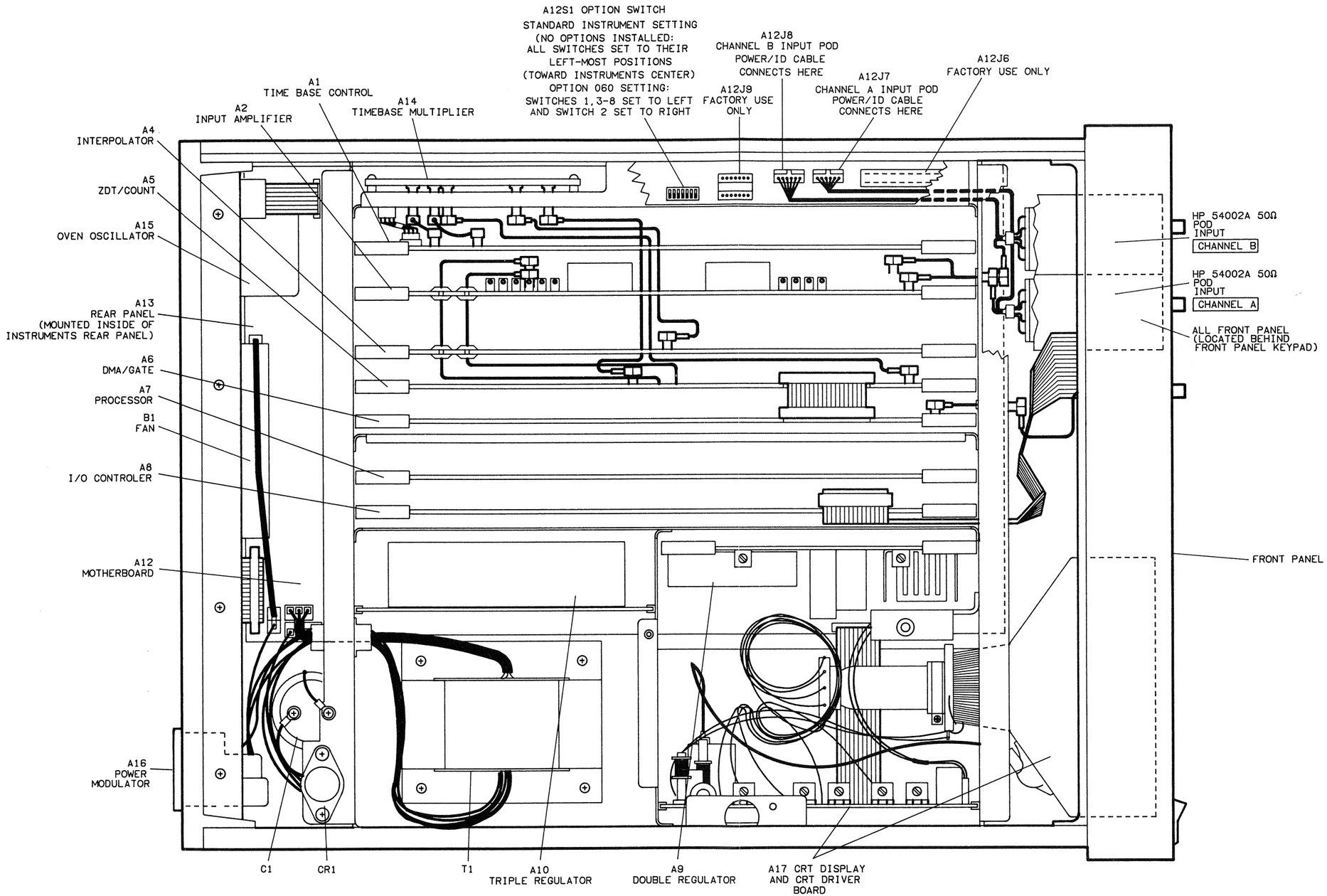


Figure 7O-1. HP 5371A Top Internal View showing Assembly Locations

7O-2. Top Cover Removal/Installation

To remove the top cover, proceed as follows:

a. Place 5371A with top cover (MP25) facing up.

b. Remove two top rear bumpers (H9) from rear of 5371A.

c. Loosen the recessed Pozidriv screw (Metric screw, HP Part Number 0515-1245) at the rear of the top cover. The screw is retained by a clip-ring (Metric, HP Part Number 0510-1253).

d. Slide the cover toward the rear of the instrument (about 1/4 of an inch) and lift off.

e. The replacement procedure is essentially the reverse of the removal procedure.

7O-3. Bottom Cover Removal/Installation

NOTE

The four feet attached to the bottom cover do not need to be removed to remove the bottom cover. However, if the feet have been removed, they should be reattached to the bottom cover BEFORE the cover is reinstalled on the instrument.

To remove the bottom cover, proceed as follows:

a. Turn the HP 5371A on its side.

b. Remove two bottom rear bumpers (H9) from rear of 5371A.

c. Loosen the the recessed Pozidriv screw (Metric screw, HP Part Number 0515-1245) at the rear of the bottom cover.

d. Slide the bottom cover to the rear until it can be lifted off.

e. The replacement procedure is essentially the reverse of the removal procedure.

7O-4. Side Cover Removal/Installation

a. Place the 5371A with the targeted side cover (MP29) facing up.

b. Remove rear bumper (H9) on the same side to have side cover removed.

c. Remove two Pozidriv screws (H8) that secure the side cover (MP29), strap handle (MP24), and front and rear strap handle caps (MP22 and MP23) to the 5371A.

d. Remove front and rear strap handle caps (MP22 and MP23 respectively).

e. Remove strap handle (MP24). Note that the strap handle is installed with its curved surface facing inward toward the instrument. (The "curved surface" has a groove that is visible when viewed from each end.)

f. Remove instrument side cover (MP29) by pulling it back toward rear of instrument.

g. To reinstall side cover (MP29), slide end with ventilation holes from rear to front of instrument until firmly seated in gap between front frame (MP16) and side struts (MP18). Push side cover (MP29) from rear until its folded end is snug against rear frame (MP17) of instrument.

h. Position strap handle (MP24), with its curved surface facing the instrument, over the threaded holes in front and rear frames.

i. Slide rear strap handle cap (MP23) onto end of strap handle (MP24) closest to rear of instrument. Ensure that concave screw guide of rear strap handle cap is aligned with slot in side strap metal and threaded hole in rear panel. (When aligned properly, the rear strap handle cap should "snap" into place.)

j. Secure in place using Pozidriv screw H8. DO NOT tighten at this time.

k. Slide front strap handle cap (MP23) into groove in side panel toward front of instrument. Adjust until the front strap handle cap screw guide is aligned with slot in side handle and threaded hole in front frame, and its two plastic ears are seated firmly against and under the front frame of the instrument.

l. Secure front strap handle cap in place with another Pozidriv screw (H8). DO NOT tighten at this time.

m. Check to see if strap handle is secure and doesn't bind against screws.

n. Tighten down both screws (H8).

7O-5. Front Panel Assembly Removal/Installation

The removal of the Front-panel assembly, which is comprised of the plastic front panel (MP8) and metal front frame (MP16), must be removed to gain access to the CRT assembly, STBY-ON power switch, front-panel keypad (MP9), and A11 front-panel printed circuit board HP Part Number 05371-60011). Proceed as follows:

a. Remove the top (MP25), bottom (MP28) and both instrument side covers (MP29) as described in the appropriate paragraphs.

WARNING

DO NOT REMOVE THE INTERNAL POWER SUPPLY COVER (MP7) WITH AC POWER CONNECTED TO THE HP 5371A. DISCONNECT POWER CABLE FROM INSTRUMENT IF YOU HAVE NOT DONE SO ALREADY. REMEMBER, UP TO 12 KILOVOLTS IS PRESENT WITHIN THE POWER SUPPLY CAVITY WHEN THE INSTRUMENT IS CONNECTED TO AN AC SOURCE.

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b. Remove internal power supply cover (MP7). This cover is located on the left-hand side as you face the instrument.

c. Remove metal CRT Driver Board bracket (MP30) by removing two Pozidriv screws (H31). This allows the CRT Driver Board to move along the two plastic card guides for easier access to cabling or for removal of the board altogether.

NOTE

Make note of the plastic card guide riveted to the CRT Driver Board bracket (MP30). When reassembling, ensure that the CRT Driver Board edge is within the groove of this card guide.

d. Disconnect the following CRT Display-CRT Driver Board interconnect cables as follows:

NOTE

The single red anode cable connects to the CRT via a compression type fitting. To ensure that all the electrical charge on the CRT display unit itself has dissipated, short the point of cable-CRT display connection to the HP 5371A chassis.

1. Disconnect single anode cable (RED) from the CRT display using a pair of long-nose pliers.
2. Disconnect six video control cables from CRT via polarized ceramic connector.
3. Disconnect two horizontal control cables (BRN and YEL) from 3-pin connector of the CRT Driver Board.
4. Disconnect two vertical control cables (RED and BLU) from 2-pin connector of the CRT Driver Board.
5. Disconnect single ground cable (GRN) from the CRT Driver Board.
6. If the CRT Driver Board is being removed from the instrument along with the CRT Display for replacement, disconnect the six-wire flat ribbon cable from A12 Motherboard connector J1 and remove printed circuit board from instrument. (It may be necessary to remove A10 Triple Regulator Board to gain access to the A12J1 connector.)

e. If this HP 5371A is equipped with Option 060, Rear Panel Inputs, skip to Step J. For Option 060 units, Step F through I may be omitted since such units are not equipped with input pods and both input channels and external arm channel are enter through the rear panel.

f. Remove both HP 54002A Input Pods by rotating the captive knurled head screw found on each, in the counterclockwise direction.

g. Gaining access from bottom of instrument, remove pod cables (W23, W24) from MP32 probe guide slots by removing four Pozidriv screws (H3). Use a 1-point Pozidriv screwdriver. Make note of which cable goes to what pod.

h. Remove two screws (H5) that secure pod cover (MP33) to card cage assembly (MP2).

i. Using an 6 (mm or in) open-end wrench, disconnect "External Arm" cable W21 from the W6 cable at the front bulkhead connector where the two cables are joined. Cable W21 routes the "External Arm" signal from the front panel input to the bulk head connector in all HP 5371A standard units.

j. Disconnect 32-conductor flat ribbon cable (W5) from A11 Front Panel Board connector J1.

k. Place HP 5371A on its rear panel.

l. Remove screws (H11) and (H12) that secure front panel (MP8) to the four corner struts.

m. Carefully lift front panel assembly up and away from rest of instrument. Make sure all cables are free of any obstructions while removing front panel assembly.

n. Place the front panel face down on a flat surface. The front handles (MP26) will protect the CRT, keypad, and data entry knob during maintenance.

o. The replacement procedure is essentially the reverse of the removal procedure.

7O-6. A1 Timebase Control Board Removal/Installation

To remove the A1 board from the card cage, proceed as follows:

a. Remove instrument top cover (MP25) from the 5371A.

b. Remove RF Cavity Cover (MP5) by loosening 10 captive knurled nuts.

c. Place HP 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A1 board approximately 2 inches out of card cage, gaining access to cables.

e. Disconnect the following cable assemblies:

1. W18 Timebase Power Supply Cable
2. W13 1 MHz Reference Clock Cable: connects A1J1 to A14J7
3. W14 10 MHz Clock Cable: connects A14J5 to A1J2

f. Remove A1 assembly from card cage.

g. The A1 Timebase Control Board installation procedure is essentially the reverse of the removal procedure.

7O-7. A2 Input Amplifier Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP5) by loosening 10 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A2 assembly approximately 2 inches out of card cage, gaining access to cables.

e. Disconnect the following cables:

1. A5W1 Count Cable Assembly: connects A2J2 to A5W1. A5W1 is a fixed part of the A5 ZDT/Count Board.
2. A5W2 Count Cable Assembly: connects A2J4 to A5W1. A5W2 is a fixed part of the A5 ZDT/Count Board.
3. W19 Pod Cable Assembly: connects front bulkhead connection with A2J1.
4. W20 Pod Cable Assembly: connects front bulkhead connection with A2J3.

f. Remove A2 assembly from card cage.

g. The A2 Input Amplifier Board installation procedure is essentially the reverse of the removal procedure.

7O-8. A4 Interpolator Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP5) by loosening 10 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A2 assembly approximately 2 inches out of card cage, gaining access to cables.

e. Disconnect the W16 500 MHz Clock Cable. W16 connects A14J9 to A4J2.

f. Remove A4 assembly from card cage.

g. The A4 Interpolator Board installation procedure is essentially the reverse of the removal procedure.

7O-9. A5 ZDT/Count Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP5) by loosening 10 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A5 assembly approximately 2 inches out of card cage, gaining access to cables.

e. Disconnect the following cables:

1. Timebase Power Supply (W18)
2. 1 MHz Reference Clock – connects A1J1 to A14J7 (W13)
3. 10 MHz Clock – connects A1J2 to A14J5 (W14)

f. Remove A1 assembly from card cage.

g. The A1 Timebase Control Board installation procedure is essentially the reverse of the removal procedure.

7O-10. A6 DMA/Gate Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP31 or MP5) by loosening 10 captive knurled nuts.

c. Place HP 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A1 board approximately 2 inches out of card cage, gaining access to cables..

e. Disconnect the following cables:

1. Timebase Power Supply (W18)
2. 1 MHz Reference Clock – connects A1J1 to A14J7 (W13)
3. 10 MHz Clock – connects A1J2 to A14J5 (W14)

f. Remove A1 assembly from card cage.

g. The A1 Timebase Control Board installation procedure is essentially the reverse of the removal procedure.

7O-11. A7 Processor Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove Power Supply Cover (MP7) by loosening 6 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A7 assembly approximately 2 inches out of card cage, gaining access to cables.

e. Remove A7 assembly from card cage.

f. The A7 Processor Board installation procedure is essentially the reverse of the removal procedure.

7O-12. A8 I/O Controller Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove Power Supply Cover (MP7) by loosening 6 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A8 assembly approximately 2 inches out of card cage, gaining access to cables.

e. Disconnect the W5 Front Panel Cable Assembly. W5 connects A8J1 to A11J1.

f. Remove A8 assembly from card cage.

g. The A8 I/O Controller Board installation procedure is essentially the reverse of the removal procedure.

7O-13. A9 Double Regulator Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove Power Supply Cover (MP7) by loosening 6 captive knurled nuts.

c. Place 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A9 assembly out of the XA9 slot.

e. The A9 Double Regulator Board installation procedure is essentially the reverse of the removal procedure.

7O-14. A10 Triple Regulator Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP7) by loosening 6 captive knurled nuts.

c. Place the 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A10 assembly out of its XA10 slot.

e. Remove A1 assembly from card cage.

f. The A10 Triple Regulator Board installation procedure is essentially the reverse of the removal procedure.

7O-15. A11 Front Panel Board Removal/Installation

a. Remove instrument top cover (MP25).

b. Remove RF Cavity Cover (MP31 or MP5) by loosening 10 captive knurled nuts.

c. Place HP 5371A on its left side (as viewed from the front).

d. Using nylon board extractor ears, pull A1 board approximately 2 inches out of card cage, gaining access to cables..

e. Disconnect the following cables:

1. Timebase Power Supply (W18)
2. 1 MHz Reference Clock – connects A1J1 to A14J7 (W13)
3. 10 MHz Clock – connects A1J2 to A14J5 (W14)

f. Remove A1 assembly from card cage.

g. The A1 Timebase Control Board installation procedure is essentially the reverse of the removal procedure.

7O-16. A13 Rear Panel Board Removal/Installation

a. Remove top and bottom covers (MP25 and MP28).

b. Remove A15 Oven Oscillator Assembly.

c. Remove six hex nuts (H25) and lock washers (H20) that secure the A13 Rear Panel Board to the rear panel (MP6). Use a 9/16 inch deep-well (0.75 inch) Hex Nut Driver or a 9/16 inch open-end wrench.

d. Remove A13 printed circuit board from HP 5371A chassis.

e. The A13 Rear Panel Board installation procedure is essentially the reverse of the removal procedure.

7O-17. A14 Timebase Multiplier Board Removal/Installation

a. Remove top cover (MP25) of the HP 5371A.

b. Remove right-hand side cover (MP29) (as viewed from the front of the instrument).

c. Remove 20 screws (H10) secure the A14 assembly cover in place.

d. Remove 2 remaining screws (H7) from cover.

e. Remove metal frame (MP31) from around the assembly.

f. Using the 6 mm open-end wrench, untighten connectors J8, J9, J11. Gain access to these connectors from the top of instrument.

g. Gently disengage A14 assembly from connectors, paying close attention to the two additional connectors, J5 and J7, located at the bottom of the instrument.

h. To reassemble, install board carefully ensuring four chassis-mounted feedthrough cap (C2-C5) posts enter A14 connectors J1 to J4 without bending.

i. Tighten connectors J8, J9, and J11 snug with fingers then tighten securely with 6 mm open-end wrench.

j. Hold metal frame and cover in its proper place.

k. Install one screw (H20) at each corner. Do not tighten at this time.

l. Install two screws (H7) located at center of cover. Again, do not tighten at this time.

m. Install remaining sixteen screws (H20) at this time.

n. Tighten down all screws.

7O-18. A15 Oven Oscillator Assembly Removal/Installation

a. Remove top and bottom covers, MP25 and MP28.

b. Disconnect coaxial cable (W3) from A13 Rear Board connector A13J1.

c. Locate the two 6-32 screws on either side of connector A12XA15 on the left-rear side of the A12 Motherboard. These two screws secure the A15 Oven Oscillator assembly to the A12 Motherboard.

d. Using a 2-point Pozidriv screwdriver, remove the two screws (H22).

e. Gently remove the oscillator assembly from connector A12XA15, gaining access from the top of instrument. Apply even force as you remove it from connector A12XA15 to prevent damage to either the A12XA15 or the 15-pin printed circuit board connector.

f. The A15 Oven Oscillator installation procedure is essentially the reverse of the removal procedure.

7O-19. B1 Cooling Fan Removal/Installation

To remove the cooling fan (B1), proceed as follows:

a. Remove instrument top cover (MP25).

b. Disconnect fan cable (W8) from A12 Motherboard connector J4.

c. With one hand, secure fan in place.

d. With the other hand, remove four screws (H18) that secure both the fan (B1) and fan guard (MP14) to the rear panel (MP6).

e. Remove fan from chassis.

f. Remove fan cable (W8) from old fan and place it on new one.

g. The cooling fan (B1) installation procedure is essentially the reverse of the removal procedure.

NOTE

When installing the new cooling fan, remember that air is drawn into the HP 5371A through the rear panel. When viewed from the rear panel, the fan will rotate in clockwise direction. Also, the point of connection of cable W8 to the fan is the upper-left hand corner of the instrument (as viewed from the HP 5371A rear panel).

7O-20. Field Installation Procedure for Option 060

The following procedure describes how to install Option 060, Rear Panel Inputs, into a standard HP 5371A equipped with front panel inputs. Proceed as follows:

Obtain the Option 060 Rear Panel Input Parts listed below:

- W10 CHANNEL A Rear Input Cable (HP Part No. 05371-60208, Qty 1)
- W11 CHANNEL B Rear Input Cable (HP Part No. 05371-60208, Qty 1)
- W12 EXTERNAL ARM Rear Input Cable (HP Part No. 05371-60215, Qty 1)
- MP33 Blank Front-panel Pod Covers (HP Part No. 54100-64101, Qty 2)
- MP38 Cable Clamps (HP Part No. 1400-1231, Qty 5)
- H20 Lock Washers (HP Part No. 2190-0102, Qty 3)
- H25 Hexagonal Nuts (HP Part No. 2950-0035, Qty 3)
- H29 Front-Panel EXTERNAL ARM Hole Plug (HP Part No. 05371-20205, Qty 1)

Tools Required:

5/16" Open-end Wrench
9/16" Nut Driver (Deep-well)
2-Point (Large) Pozidriv Screwdriver
6 mm Open-end Wrench

Install Option 060 as follows:

a. Disconnect AC power cable from HP 5371A rear panel.

b. Remove instrument top cover (MP25).

c. Remove right side cover (MP29) of instrument (as viewed from the front panel).

d. Using the appropriate tool (i.e., needle-nose pliers), bend the metal pins securing the the three metal hole plugs (H28) to the Option 060 rear panel CHANNEL A, CHANNEL B, and EXTERNAL ARM holes of the HP 5371A.

e. Remove both input pods installed in the front panel (i.e., HP 54001A, 54002A, or 54003A). Also remove W23 and W24 Pod Power/ID cables. Front panel input pods and associated cabling cannot be used when Option 060 is installed.

f. Remove front-panel W9 EXTERNAL ARM input cable. Install H29 Front-panel EXTERNAL ARM Hole Plug where W9 BNC connector was installed.

g. Install two blank pod covers (MP33) in front panel input pod slots, using the knurled nut to secure each cover to instrument.

h. Attach five cable clamps MP38, to the instrument chassis as follows:

1. Attach one cable clamp to the upper-right corner of the card cage. (See
2. Attach two cable clamps to the inner side of the right-corner strut, spacing them approximately two inches apart.
3. Attach remaining two cable clamps toward the top of card cage's side, spacing them two to three inches apart.

i. Install EXTERNAL ARM Rear Panel Input Cable, W12, as follows:

1. From inside the instrument, insert W12 cable BNC RF connector through rear-panel EXTERNAL ARM hole.
2. Secure cable's BNC RF connector to rear panel using lock washer (H20) and hexagonal nut (H25). Tighten hex nut using 9/16" Nut Driver.
3. Route cable from rear to front of instrument. Secure cable into the five cable clamps installed earlier.
4. Connect W12 cable's right-angle SMB connector to W21 External Arm Extension Cable bulkhead connector which is secured to front of card cage. Tighten connector until snug using 6 mm open end wrench.

j. Install CHANNEL A Rear Panel Input Cable, W10, as follows:

1. From inside the instrument, insert W10 cable BNC RF connector through rear-panel CHANNEL A hole.
2. Secure cable's BNC RF connector to rear panel using lock washer (H20) and hexagonal nut (H25). Tighten hex nut using 9/16" Nut Driver.
3. Route cable from rear to front of instrument. Secure cable into the five cable clamps installed earlier.
4. Connect W10 cable's right-angle SMA connector to W19 CHANNEL A Input Extension Cable bulkhead connector which is secured to front of card cage. Tighten down until snug using 5/16" open-end wrench.

k. Install CHANNEL B Rear Panel Input Cable, W11, as follows:

1. From inside the instrument, insert W11 cable BNC RF connector through rear-panel CHANNEL B hole.
2. Secure cable's BNC RF connector to rear panel using lock washer (H20) and hexagonal nut (H25). Tighten hex nut using 9/16" Nut Driver.
3. Secure cable into the five cable clamps installed earlier.
4. Connect W11 cable's right-angle SMA connector to W20 CHANNEL B Input Extension Cable bulkhead connector which is secured to front of card cage. Tighten down until snug using 5/16" open-end wrench.

l. When a standard instrument is shipped from the factory, the Option 060 Selection Switch (A12S1) is set with all eight switches in their left-most position (i.e. toward center line of instrument as viewed from the front panel). To modify switch settings to accommodate installation of Option 060, set switch #2 (i.e., second switch from the instrument's front panel) to its right-most position (away from instument's center line as viewed from front panel).

SECTION 7P
SIGNALS

Table 7P-1 is a list signals used in the 5371A. The list is arranged in alphanumeric order and includes signal name, logic level, source, destination, and brief description. The signal name is listed as it appears on the schematics for easy cross-referencing. *Figure 7P-1* (the foldout located at the end of this section) shows the A12 Motherboard pinout configuration as viewed from the bottom (circuit side) of the board.

Table 7P-1. 5371A Signals

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
10_MHz_REF	0.55 ±0.05 V rms into 50 Ohms. 1V rms ±20% into 1K Ohm load.	A12XA15(1,16)	A12XA1H(1)	10_MHz_REF is the internal timebase frequency generated by the A15 Oven Oscillator and used to generate the two 500 MHz reference frequencies, CLKA and CLKB.
+10VA	+10V ±0.5 V dc (Nominal)	A12XA1A(38)	A12J7(1) A12J6(35)	Regulated +10V dc power supply for the Channel A Input Pod. (Used only by 54001A and 54003A Input Pods.)
-10VA	-10V ±0.5V dc (Nominal)	A12XA1A(15)	A12J7(6) A12J6(38)	Regulated -10V dc power supply for the Channel A Input Pod. (Used only by 54001A and 54003A Input Pods.)
+10VB	+10V ±0.5V dc (Nominal)	A2XA1A(41)	A12J8(1) A12J6(36)	Regulated +10V dc power supply for the Channel B Input Pod. (Used only by 54001A and 54003A Input Pods.)
-10VB	-10V ±0.5V dc (Nominal)	A12XA1A(18)	A12J8(6) A12J6(37)	Regulated -10V dc power supply for the Channel B Input Pod. (Used only by 54001A and 54003A Input Pods.)
+12CRT	+12V ± 0.6V dc, Nominal, with < 50 mV (p-p) ripple and noise.	A12U2(2)	A12J1(4)	Regulated +12V dc operating voltage for the front-panel CRT Display.
+12OSC	+11.0-+13.5V dc, (+12.0V dc Nominal, with <100 μV rms ripple and noise.)	A12U8(3)	A12XA15(3,18)	Regulated +12V dc for A15 Oven Oscillator's crystal.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
+15OSC	+15V dc (Nominal)	A12XA1B(46)	A12U8(1)	Switched +15V dc sent to +12OSC regulator A12U8. A1 Timebase Control Board applies +15V to the regulator input when 1,2,5, or 10 MHz is not connected to rear-panel EXTERNAL INPUT connector. When external reference frequency is connected to the rear panel, +12OSC is turned off, disconnecting voltage to the A15 Oven Oscillator crystal. This turns off the A15 assembly's 10 MHz output.
-15RAW	-15.01V- -14.99V dc	A12XA10B(21, 11, 26)	A12XA1A(3,28) A12XA2A(3,28) A12XA6(4) A12XA9(39)	Provides regulated -15V dc to the A1, A2, and A6 daughter boards. -15RAW is also used by the A9 Double Power Supply.
+15RAW	+14.99V- +15.01V dc	A12XA10B(6, 8, 10, 23)	A12XA1A(1,26) A12XA2A(1,26) A12XA6(6,76) A12U2(1)	Provides regulated +15V dc to the A1, A2, and A6 daughter boards. +15RAW is also used by the A12 Motherboard.
1BCLKCO	ECL	A12XA5A(43)	A12XA6(94)	Clock Carry-Out is generated by Event 1 counter ZDT1B, A5U15. 1BCLKCO, along with 2BCLKCO generated by Event 2 counter ZDT2B (A5U40), are asserted whenever the 32-bit event counters (ZDT1AB or ZDT2AB) overflow. Circuitry on A6 DMA/Gate Board provide for the detection, latching and reading by the 68000 μP of both the 1BCLKCO and 2BCLKCO signals. **NOTE:** The overflow detection circuitry is loaded on the A6 DMA/Gate Board, but the function of event counter overflow is currently performed by the 5371A software.
1BL1CO	ECL	A12XA5A(42)	A12XA6(92)	Latch 1 Carry-Out is generated by Event 1 counter ZDT1B, A5U15. This signal is used when the incoming clock, or events, are not synchronous with the measurement latch signals. A Totalize measurement is an example

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				of such a measurement. 1BL1CO and 1BL2CO, along with 2BL1CO and 2BL2CO generated by Event 2 counter ZDT2B (A5U40), are sent to the "Totalize" circuit on the A6 DMA/Gate Board for detection.
1BL2CO	ECL	A12XA5A(28)	A12XA6(95)	Latch 2 Carry-Out is generated by Event 2 counter ZDT1B, A5U15. See "1BL1CO" for additional information.
+25V	+25V to +32V dc (Unregulated)	A12J2(4)	A12XA10A(7-10,16-20) A12XA9(1-3,26,27) A12XA8(115) A12U3(3) A12U11(1) TO RESISTORS A12R12, R20, R23, R25, R2, AND R29.	+25V dc (unregulated) is derived from chassis-mounted full-wave rectifier, CR1 and C1. +25V dc provides input voltage to the A10 Triple Regulator Board, A9 Double Regulator Board, +5P Motherboard Regulator, the front-panel STANDBY LED, and is distributed to miscellaneous A12 Motherboard circuitry.
2BCLKCO		A12XA5H(59)	A12XA6(114)	Clock Carry-Out is generated by Event 2 counter ZDT2B, A5U40. See earlier description of "1BCLKCO" for details.
2BL1C0	ECL	A12XA5H(60)	A12A6(44)	Latch 1 Carry-Out is generated by Event 2 counter ZDT2B, A5U40. See earlier description of "1BL1CO" for details.
2BL2CO	ECL	A12XA5H(57)	A12XA6(43)	Latch 2 Carry-Out is generated by Event 2 counter ZDT2B, A5U40. See earlier description of "1BL1CO" for details.
-3.3RAW	-3.29V to -3.27V dc	A12XA9 (19, 21, 23, 25, 44, 46, 48, 50)	A12XA5A(2-4, 18-20, 34-36, 50-52)	Provides regulated -3.25V dc to the EFL logic components (Sequencer and six ZDT counter ICs) found on the A5 daughter board.
3BCLKCO	ECL	A12XA5A(11)	A12XA6(93)	Clock Carry-Out is generated by Timing Counter ZDT3B, A5U27. This signal is not used.
3BL1CO	ECL	A12XA5A(25)	A12XA6(18)	Latch 1 Carry-Out is generated by Timing Counter ZDT3B, A5U27. This signal is not used.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
3BL2CO	ECL	A12XA5A(10)	A12XA6(91)	Latch 2 Carry-Out is generated by Timing Counter ZDT3B, A5U27. This signal is not used.
-5.2RAW	-5.21V to -5.19V dc	A12XA9(7 ,9, 11, 13, 32, 34, 36, 38)	A12XA1A(5,6,30,31) A12XA2A(5,6,30,31) A12XA4A(5,6,30,31) A12XA5A(1,17,33,49) A12XA6(1,2,72) A12XA7(1)	Provides regulated -5.2V dc to the ECL logic components found on the A1, A2, A4, A5, A6, and A7 daughter boards.
+5RAW	+4.8V to +5.2V dc	A12XA10B(3, 7, 13, 18 ,22 ,25, 28)	A12XA1A (10,11, 35,36) A12XA2A (10,11, 35,36) A12XA4A (10,11, 35,36) A12XA5A (5, 6, 21, 22, 37 , 38 ,53 ,54) A12XA6 (11-13,82) A12XA7 (11-13,81-83) A12XA8 (11-13,81-83) A12XA9(14,15,40) +5V supplied to A11 Front Panel Board via connector A8J1(8,9).	Provides regulated +5V dc to the TTL logic components found on the A1, A2, A4, A5, A6, A7, A8, and A9 daughter boards. +5V dc is also sent to the A11 Front Panel Board to provide miscellaneous LED drive voltage.
~8_BIT_DAC_CS		A12XA1B (17)	No Connection	This signal is used exclusively on the A1 Timebase Control Board.
AC1	60V (p-p) sine wave at 60 Hz	A12J3(1)	A12J2(1) A12CR3	AC1 and AC2 are the secondary outputs of chassis-mounted transformer T1. AC1 and AC2 provide inputs to the following circuits: (1) chassis-mounted rectifier (CR1 and C1) for generation of unregulated +25V dc, (2) local rectifier (A12CR2 and A12CR3) for generation of "standby" mode back-up power (LP) for A7 assembly CMOS ICs, and (3) input to the "Power-Fail Detect" circuit located on the A12 Motherboard where it is monitored.
AC2	60V (p-p) sine wave at 60 Hz	A12J3(3)	A12J2(2) A12CR2	
ARM_DELAY 1	TTL	A12XA5H(48)	Routes to buffer A12U5A(1), then from A12U5A(3) to connector A12J10(6).	The falling edge of ARM_DELAY 1 indicates when all arming conditions for measurements using A5 ZDT/Count Board Event Counter 1 Chain have been

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				met. For example, if a time holdoff is specified, a falling edge occurs after the time holdoff is complete. ARM_DELAY 1 is available at the instrument's rear panel, informing the user when the measurement is armed.
ARM_DELAY 2	TTL	A12XA5H(63)	Routes to buffer A12U5F(19), then to connector A12J10(7).	The falling edge of ARM_DELAY 2 indicates when all arming conditions for measurements using A5 ZDT/Count Board Event Counter 2 Chain have been met. For example, if a time holdoff is specified, a falling edge occurs after the time holdoff is complete. This signal is available at the instrument's rear panel, informing the user when the measurement is armed.
~ATN	TTL	A12XA8(63)	A12J5(11)	ATtentioN is an HP-IB control line that alerts the 5371A that a device-independent message is being sent over the bus. When ATN is low (true), the HP-IB enters "Command Mode" allowing the external system controller to address the 5371A either as a talker or listener. When ~ATN is high (false), the HP-IB enters "Data Mode" and data can transfer between the 5371A and the system controller.
A_COMP	EECL	A12XA2B(44)	A12XA1B(44) A12J6(18)	Auxiliary Comparator A indicates to the 68000 μP if the CHANNEL A comparator output (A2U4) is high or low. This signal is used for setting the auto trigger level and detection of an input signal on CHANNEL A.
B(S*~T)	ECL	A12XA6(19)	A12XA5A(57)	Buffered "SINGLE and TOTALIZE NOT" is used with B(S+~T) to program the A5 ZDT/Count Board to perform single, double, or quadruple latch measurements.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
B(S+~T)	ECL	A12XA6(88)	A12XA5A(56)	Buffered "SINGLE or TOTALIZE NOT" is used with B(S*~T) to program the A5 ZDT/Count Board to perform single, double, or quadruple latch measurements.
B19.66MHz	TTL	A12XA7(2)	A12XA8(2)	The buffered version of the 19.6608 MHz system clock that runs all digital circuits on the A7 and A8 assemblies.
BA1	TTL	A12XA7(99)	A12XA8(99)	BA1-BA18 are the buffered, bidirectional System Address Lines that allow either the 68000 μP (A7U8) or DMA Controller (A8U30) to gain access to memory space. The 68000 μP can directly address the A8 assembly's "Display Memory" when temporarily storing measurement data or writing data for display on the front-panel CRT. The DMA Controller (A8U30) can also generate System RAM addresses when data is sent directly from A7 assembly's "System RAM" to the HP-IB.
BA2	TTL	A12XA7(29)	A12XA8(29)	
BA3	TTL	A12XA7(98)	A12XA8(98)	
BA4	TTL	A12XA7(28)	A12XA8(28)	
BA5	TTL	A12XA7(97)	A12XA8(97)	
BA6	TTL	A12XA7(27)	A12XA8(27)	
BA7	TTL	A12XA7(96)	A12XA8(96)	
BA8	TTL	A12XA7(26)	A12XA8(26)	
BA9	TTL	A12XA7(94)	A12XA8(94)	
BA10	TTL	A12XA7(23)	A12XA8(23)	
BA11	TTL	A12XA7(93)	A12XA8(93)	
BA12	TTL	A12XA7(22)	A12XA8(22)	
BA13	TTL	A12XA7(92)	A12XA8(92)	
BA14	TTL	A12XA7(21)	A12XA8(21)	
BA15	TTL	A12XA7(91)	A12XA8(91)	
BA16	TTL	A12XA7(89)	A12XA8(89)	
BA17	TTL	A12XA7(19)	A12XA8(19)	
BA18	TTL	A12XA7(88)	A12XA8(88)	
~BAS	TTL	A12XA7(74)	A12XA8(74)	The buffered version of the Address Strobe line is set high (false) to inform the "Bus Arbitration" circuit (located on the A8 I/O Controller Board) that the 68000 μP is not using the bus.
~BBG	TTL	A12XA7(5)	A12XA7(5)	The buffered version of the Bus Grant line is set low (true) to inform any device requesting control of the 5371A bus that the 68000 μP will relinquish bus control at the end of the current bus cycle.
~BCHAR	TTL	A12XA8(43)	No Connection	The buffered version of of the 1.2288 MHz timing control clock. ~BCHAR defines the character length of the video data transferred from the A8 I/O Controller Board to the front-panel CRT display. ~BCHAR is not used.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
BCLK	TTL	A12XA7(3)	A12XA8(3)	The buffered version of the 9.8304 MHz 68000 μP clock.
BD0	TTL	A12XA7(51)	A12XA8(51)	BD0-BD15, the buffered version of the 16-bit bidirectional System Data Bus, provides a path for unprocessed data from either the Count Hardware RAM or System RAM to the HP-IB as what occurs during a DMA cycle, and a path for processed data to the front-panel CRT. The 68000 μP also uses this path to read/write unprocessed measurement data from "Display Memory" located on the A8 assembly. The System Data Bus is isolated from the Count Hardware Data Bus by Count Hardware Buffers, A7U32 and U36, and from the 68000 μP Private Data Bus by Global Bus Buffers, A7U33 and U39. All three buses are buffered from one another on the A7 Processor Board.
BD1	TTL	A12XA7(121)	A12XA8(121)	
BD2	TTL	A12XA7(52)	A12XA8(52)	
BD3	TTL	A12XA7(122)	A12XA8(122)	
BD4	TTL	A12XA7(53)	A12XA8(53)	
BD5	TTL	A12XA7(123)	A12XA8(123)	
BD6	TTL	A12XA7(54)	A12XA8(54)	
BD7	TTL	A12XA7(124)	A12XA8(124)	
BD8	TTL	A12XA7(61)	A12XA8(56)	
BD9	TTL	A12XA7(131)	A12XA7(126)	
BD10	TTL	A12XA7(62)	A12XA8(57)	
BD11	TTL	A12XA7(132)	A12XA8(127)	
BD12	TTL	A12XA7(63)	A12XA8(58)	
BD13	TTL	A12XA7(133)	A12XA8(128)	
BD14	TTL	A12XA7(64)	A12XA8(59)	
BD15	TTL	A12XA7(134)	A12XA8(129)	
BDREQ1	TTL	A12XA8(112)	No Connection	The buffered version of DREQ1. DREQ1 is set low by the HP-IB Controller IC (A8U50) which informs the DMA Controller IC (A8U30) that it is ready to transfer a byte of data. BDREQ1 is not used.
BE	TTL	A12XA7(73)	A12XA8(73)	The buffered version of Enable signal generated by the 68000 μP that enables the Serial Port (A7U19) and CRT Controller (A8U12). BE is a peripheral control line that allows the asynchronous 68000 μP to interface with the synchronous Serial Port or CRT Controller ICs.
BFUL_W	ECL	A12XA6(29)	A12XA5A(61)	BFUL_W is set high by the A6 assembly's "DMA Measurement RAM Address Generation" circuit when the highest order address counter output buffer is full. This means the

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				last RAM address in a in a measurement, or block of measurements, is about to be placed on the address bus. BFUL_W informs the A5 ZDT/Count Board that one more write cycle is left in the current measurement. After a delay of one clock cycle, BFUL_W generates RAMTC which informs the 68000 μP that the last set of measurement data has been loaded into count hardware memory.
~BGACK	TTL	A12XA8(76)	A12XA7(76)	Bus Grant ACK, generated by the A8 I/O Controller Board "Bus Arbitration Circuit", informs the 68000 μP that the DMA Controller IC now controls the System Bus.
~BGDT1 ~BGDT2 ~BGDT3	TTL TTL TTL	A12XA7(16) A12XA7(85) A12XA7(15)	A12XA8(16) A12XA8(85) A12XA8(15)	~BGDT1-~BGDT3, the buffered version of Generate Data Transfer acknowledge, is set low to generate the System Bus DTACK signal. DTACK is expected when each decoded address is placed on the on the System Bus. The numeric portion of the alphanumeric signal name (i.e., the "2" of "~BGDT2") represents bus cycle time in hundreds of nanoseconds. Using ~BGDT2 to generate DTACK generates a bus cycle 200 ns in length (2 * 100 = 200 ns).
~BGDT5	TTL	A12XA7(79)	No Connection	Not Used
BGR/~W	TTL	A12XA7(105)	A12XA8(105)	The buffered version of bi-directional Gated Read/~Write signal clocks data during all "write" cycles. This signal is generated by either the A7 Processor Board's 68000 μP (A7U8) and 'Timing Signal Generation and Synchronization" circuit or the A8 I/O Controller Board's DMA Controller (A8U30). BGR/~W is active (low) whenever the 68000 μP writes to any memory location,

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				and is inactive (high) when it reads from any memory location. BGR/~W is set low (active) by Data Strobe, ~DS. ~DS is active (low) whenever valid data is on the data bus. BGR/~W goes high after the 68000 μP has received a DTACK signal, indicating that the write cycle is over. The BGR/~W generated by the DMA Controller is inactive (high) when data is read from either the System RAM or Measurement RAM to the HP-IB port. ~CTWR, a Count Hardware Bus control signal, is a buffered version of BGR/~W.
BHSYNC	TTL	A12XA8(38)	A12J6(22)	The buffered version of Horizontal SYNChronization line is used for in-factory test purposes only.
~BIACK	TTL	A12XA7(75)	No Connection	The buffered version of the Interrupt ACKnowledge line is not used.
~BLDS	TTL	A12XA7(107)	A12XA8(107)	The buffered version of the Lower Data Strobe line is a bidirectional signal that determines if the bus cycle currently in progress is accessing the lower byte of a 2-byte word. The 68000 μP or the DMA Controller IC can generate the ~BLDS depending on which IC has control of the 5371A bus.
BMA13	TTL	A12XA8(45)	No Connection	The buffered version of Display Memory address line MA13, is one of 14 address lines that can access up to 16K words of CRT Display memory. BMA13 is not used.
~BMEAS	ECL	A12XA6(32)	A12XA5A(62)	The buffered version of the measurement control word ~MEAS bit. ~BMEAS' main function is to turn on and off the A6 DMA/Gate Board's DMA circuitry. When set low (true), a measurement is in progress. When set high

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				(false) the "Initialization" circuit of the A5 ZDT/Count effectively stops the counting hardware and permits processing of the measurement data.
~BR	TTL	A12XA8(6)	A12XA7(6)	The Bus Request line is is set low when the DMA Controller A8U30 needs control of the 5371A bus.
BR/~W	TTL	A12XA7(36)	A12XA8(36)	The buffered version of the R/~W line is a bidirectional control line that allows either the 68000 μP (A7U8) or the DMA Controller (A8U30) to inform the 5371A circuitry that either a read or write cycle is in progress.
~BREAD	TTL	A12XA7(106)	A12XA8(106)	The buffered version of the READ signal is a bidirectional signal that is set low (true) when data is read from the count hardware Measurement RAM. ~BREAD is set low until the appropriate DTACK signal has been returned, indicating that the data has been read by either the 68000 μP (A7U8) or DMA Controller (A8U30). ~CTRD, a Count Hardware Bus control signal, is a buffered version of ~BREAD.
~BROWSEL0	TTL	A12XA8(108)	No Connection	The buffered version of ~ROWSELect 0 is 1 of 4 lines used to scan the front-panel keypad for data entry detection. ~BROWSEL0 is not used.
~BS0	TTL	A12XA7(9)	No Connection	Board Select 0 is not used.
~BS1	TTL	A12XA7(78)	No Selection	Board Select 1 is not used.
~BS2	TTL	A12XA7(8)	No Selection	Board Select 2 is not used.
~BS3	TTL	A12XA7(77)	A12XA8(77)	Board Select 3 allows the decoding of address lines A16 through A18 for selection of digital circuit blocks on the A8 I/O Controller Board.
BTTR	TTL	A12XA6(79)	A12J6(28)	The buffered version of Timing TRigger signal. BTTR is used for in-factory testing only. See TTR for description.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~BUDS	TTL	A12XA7(37)	A12XA8(37)	The buffered Upper Data Strobe is a bidirectional signal that determines if the bus cycle currently in progress is accessing the upper byte of a 2-byte word. The 68000 μP or the DMA Controller IC can generate the ~BUDS depending on which IC has control of the bus.
~BUFEN0	TTL	A12XA6(101)	A12XA5A(13)	BUFfer ENable 0 line selects transceivers A5U18 and U21 allowing data to be written to counter ZDT1A (A5U22) or read from the event RAMs A5U17 and U19. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.
~BUFEN1	TTL	A12XA6(27)	A12XA5A(44)	BUFfer ENable 1 line selects transceivers A5U6 and U16 allowing data to be written to counter ZDT1B (A5U15) or read from event RAMs A5U10 and U13. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.
~BUFEN2	TTL	A12XA6(112)	A12XA5H(53)	BUFfer ENable 2 line selects transceivers A5U37 and U39 allowing data to be written to counter ZDT2A (A5U30) or read from event RAMs A5U36 and U38. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.
~BUFEN3	TTL	A12XA6(113)	A12XA5H(56)	BUFfer ENable 3 line selects transceivers A5U42 and U46 allowing data to be written to counter ZDT2B (A5U40) or read from event RAMs A5U41 and U44. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~BUFEN4	TTL	A12XA6(103)	A12XA5A(14)	BUFfer ENable 4 line selects transceivers A5U26 and U34 allowing data to be written to counter ZDT3A (A5U28) or read from Timing RAMs A5U24 or U32. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.
~BUFEN5	TTL	A12XA6(23)	A12XA5A(27)	BUffer ENable 5 line selects transceivers A5U25 and U33 allowing data to be written to Timing Counter ZDT3B or read from Timing RAMs A5U23 and U31. These transceivers gate data between the A5 ZDT/Count Board's data bus and the Count Hardware Data Bus on the A12 Motherboard.
~BVMA	TTL	A12XA7(4)	A12XA8(4)	The buffered version of the Valid Memory Address line is a peripheral control signal that allows synchronous M6800 devices to interface with the asynchronous 68000 μP. ~BVMA is generated in response to receiving a ~VPA from a MC6800 family device. When set low, this line informs the M6800 devices that a valid address is on the address bus and that the 68000 μP is ready to transfer data using the E clock for synchronization.
BVON	TTL	A12XA8(44)	A12J6(23)	Buffered version of VON, which is set high whenever a serial data stream is present at the outputs of either Video Signal Driver shift register, A8U14 or U22. BVON is used for in-factory test purposes.
BVSYNC	TTL	A12XA8(118)	A12J6(24)	The buffered version of VSYNC is used for in-factory test purposes only.
B_COMP	EECL	A12XA2B(45)	A12XA1B(45) A12J6(17)	Auxiliary Comparator B line indicates to the 68000 μP if the CHANNEL B comparator output (A2U15) is high or low.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				This signal is used for setting the auto trigger level and detection of an input signal on CHANNEL B.
C_CHAN_IN	TTL	A12J9(11)	A12XA1A(49)	Not Used
C_DETECT	TTL	A12J9(5)	A12XA1A(24)	Not Used
~CHACCESS	TTL	A12XA8(114)	No Connection	Not Used
CHDCLK	TTL	A12XA7(43)	A12XA6(56)	Count Hardware Dma CLocK signal, which is derived by the A7 Processor Board's "Count Hardware Decoding and Dump Mode Logic" circuit, increments the A6 DMA/Gate Board's Dump Mode Counter (A6U20) during a read of measurement data from the A5 ZDT/Count and A4 Interpolator Board memory locations. The number of clock pulses per read depends on the type of measurement made. CHDCLK is active only during DMAs from the counting hardware.
~CHDMA	TTL	A12XA8(113)	A12XA7(113) A12XA6(126)	Count Hardware Direct Memory Access signal enables the A6 DMA/Gate Board's Dump Mode Counter IC (A6U20) during binary dump mode. ~CHDMA is also routed to the A7 Processor Board's "Count Hardware Decoding and Dump Mode Logic" circuit. If ~CHDMA and ~BREAD are set low (true), the "Count Hardware Buffers" are turned on.
~CHDTK	TTL	A12XA6(53)	A12XA7(109) A12XA1B(6) A12U1(18)	Count Hardware Data Transfer acKnowledge is the DTACK signal for the Count Hardware Bus. ~CHDTK informs the 68000 μP that the data written to the count hardware has been accepted, or that the data to be read is valid. If after performing a read or write operation and the 68000 μP does not receive a ~CHDTK within ~60 us, a bus error will occur. ~CHDTK can be generated by either the A1

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				Timebase Control Board, A6 DMA/Gate Board, or the Option Switch buffer IC, A12U1. All three sources are wire-ORed on the A12 Motherboard.
CH_A_CONTROL	1 mV to 15 mV RMS	A12XA2A(24)	A12J6(14)	The CHannel A CONTROL signal is adjusted for minimum ac voltage level by potentiometer A2R3. This adjustment, Input Bias Loop Adjustment, cancels the effects of any input bias current at input pin 2 of DC Offset Hybrid, A2U2. CH_A_CONTROL is used for test purposes only.
CH_B_CONTROL	1 mV to 15 mV RMS	A12XA2A(48)	A12J6(15)	The CHannel B CONTROL signal is adjusted for minimum ac voltage level by potentiometer A2R1. This adjustment, Input Bias Loop Adjustment, cancels the effects of any input bias current at pin 2 of DC Offset Hybrid, A2U14. CH_B_CONTROL is used for test purposes only.
CI1	ECL	A12XA4E(1)	A12XA5K(1)	CI1 is synchronized with the 500 MHz reference frequency (CLKA) by the A4 Interpolator Board's Interpolator 1 (Start) circuit. CI1 then latches the integral counter value of 2 ns pulses currently in the Timing Counter (ZDT3AB) into memory. The integral time interval is calculated by finding the difference between count values latched by CI1 and CI2.
CI2	ECL	A12XA4D(1)	A12XA5J(1)	CI2 is synchronized with the 500 MHz reference frequency (CLKA) by the A4 Interpolator Board's Interpolator 2 (Stop) circuit. CI2 then latches the integral counter value of 2 ns pulses currently in the TIming Counter (ZDT3AB) into memory. The intergral time interval is calculated by finding the difference between count values latched by CI1 and CI2.
CLK10	TTL	A12XA1B(35)	A12XA6(117)	CLK10 is a 10 MHz clock signal that is derived from the

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				A14 Timebase Multiplier Board's 10 MHz output. The 10 MHz exits A14, is buffered by A1 Timebase Control Board, and then routed to the A6 DMA/Gate Board where it is used as the System Timer Controller (A6U41) timebase reference. CLK10 is also gated and translated into the ECL10MHZ signal.
CTA1	TTL	A12XA7(104)	A12XA1B(20) A12XA6(122)	CTA1-CTA8 are the buffered Count Hardware Address lines that enable the 68000 μP to access all count hardware locations. These lines provide address and logic control for the A1 Timebase Control and A6 DMA/Gate Boards. PAL ICs on each assembly provide logic decoding that provide address and logic control for A2 Input Amplifier and A5 ZDT/Count Boards respectively. During access of the count hardware, CTA1-CTA8 remain enabled, but remain disabled during the direct memory access (DMA) process.
CTA2	TTL	A12XA7(34)	A12XA1B(4) A12XA6(51)	
CTA3	TTL	A12XA7(103)	A12XA1B(19) A12XA6(121)	
CTA4	TTL	A12XA7(33)	A12XA1B(3) A12XA6(49)	
CTA5	TTL	A12XA7(102)	A12XA1B(39) A12XA6(119)	
CTA6	TTL	A12XA7(32)	A12XA1B(38) A12XA6(48)	
CTA7	TTL	A12XA7(101)	A12XA1B(37) A12XA6(118)	
CTA8	TTL	A12XA7(31)	A12XA1B(36) A12XA6(47)	
~CTCS1	TTL	A12XA7(138)	A12XA1B(16)	Count Hardware Chip Select 1 selects PAL IC A1U21 that is located on the A1 Timebase Control Board.
~CTCS2	TTL	A12XA7(139)	No Connection	Not Used
~CTCS3	TTL	A12XA7(70)	No Connection	Not Used
~CTCS4	TTL	A12XA7(69)	No Connection	Not Used
~CTCS5	TTL	A12XA7(68)	No Connection	Not Used
~CTCS6	TTL	A12XA7(67)	A12XA6(139)	Count Hardware Chip Select 6 selects PAL ICs A6U16, U17, U36, and U55 that are located on the A6 DMA/Gate Board. CTCS6 also clocks flip-flop A6U56B whose output is the Count Hardware DTACK signal (~CHDTK).

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~CTCS7	TTL	A12XA7(137)	A12U1(19)	Count Hardware Chip Select 7 enables Option Switch (A12S1) buffer A12U1 allowing the 68000 μP to read the instrument's Option Switch setting. This occurs at instrument power-up only. The buffer is disabled after the switch setting is read.
CTD0	TTL	A12XA7(116)	A12XA2B(8) A12XA5H(7)	CTD0-CTD15 comprise the Count Hardware Data Bus. This bus is 16-bit bidirectional bus that routes the raw measurement data from the count hardware (ZDT counter and Interpolator results) to the digital hardware for processing and display, or straight to the HP-IB port which occurs during a DMA dump. CTD0-CTD15 are buffered from the System Data Bus by Count Hardware Buffers located on the A7 assembly. The 68000 μP also uses this data bus to send control words to (1) program the Sequencer and ZDT counter ICs prior to each measurement, (2) select input signal termination bias, (3) set input signal trigger level, (4) provide input relay control, (5) and enable front-panel CHANNEL A trigger LEDs. Finally, this data bus allows the 68000 μP to determine front-panel input pod identification, status of the A1 assembly, and which options are loaded in the instrument.
		A12XA1B(8) A12XA5H(7) A12U1(17)	A12XA7(116)	
CTD1	TTL	A12XA7(46)	A12XA2B(24) A12XA5H(23)	
		A12XA1B(24) A12XA5H(23) A12U1(16)	A12XA7(46)	
CTD2	TTL	A12XA7(117)	A12XA2B(9) A12XA5H(8)	
		A12XA1B(9) A12XA5H(8) A12U1(15)	A12XA7(117)	
CTD3	TTL	A12XA7(47)	A12XA2B(25) A12XA5H(24) A12XA7(47)	
		A12XA1B(9) A12XA5H(24) A12U1(14)		
CTD4	TTL	A12XA7(118)	A12XA1B(10) A12XA5H(9) A12XA7(118)	
		A12XA2B(10) A12XA5H(9) A12U1(13)		
CTD5	TTL	A12XA7(48)	A12XA2B(26) A12XA5H(25)	
		A12XA1B(26) A12XA5H(25) A12U1(12)	A12XA7(48)	

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
CTD6	TTL	A12XA7(119)	A12XA2B(11) A12XA5H(10)	
		A12XA1B(11) A12XA5H(10) A12U1(11)	A12XA7(119)	
CTD7	TTL	A12XA7(49)	A12XA2B(27) A12XA5H(26)	
		A12XA1B(27) A12XA5H(26)	A12XA7(49)	
CTD8	TTL	A12XA7(126)	A12XA2B(12) A12XA5H(11)	
		A12XA5H(11)	A12XA7(126)	
CTD9	TTL	A12XA7(56)	A12XA2B(28) A12XA5H(27)	
		A12XA5H(27)	A12XA7(56)	
CTD10	TTL	A12XA7(127)	A12XA2B(13) A12XA5H(12)	
		A12XA5H(12)	A12XA7(127)	
CTD11	TTL	A12XA7(57)	A12XA2B(29) A12XA5H(28)	
		A12XA5H(28)	A12XA7(57)	
CTD12	TTL	A12XA7(128)	A12XA5H(42)	
CTD13	TTL	A12XA7(58)	A12XA5H(43)	
CTD14	TTL	A12XA7(129)	A12XA5H(44)	
CTD15	TTL	A12XA7((59)	A12XA5H(45)	
~CTDS	TTL	A12XA7(112)	No Connection	Not Used
~CTDT1	TTL	A12XA7(38)	A12XA6(123)	Count hardware DTacK 1 is used by the A6 assembly's count hardware to generate the ~CTDTK signal. The "1" refers one 100 ns delay from when the bus is stable to when ~CTDT1 is set low.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~CTDT3	TTL	A12XA7(108)	A12XA1B(5)	Count hardware DTacK 3 is used by the A1 Timebase Control Board's count hardware to generate the the ~CTDTK signal. The "3" refers to three 100 ns delays from when the bus is stable to when ~CTDT3 is set low.
CTR/~W	TTL	A12XA7(111)	A12XA1B(22) A12XA6(54)	CounT R/~W is a buffered version of BR/~W signal. CTR/~W informs the A1 Timebase Control and A6 DMA/Gate Boards that a count hardware read or write cycle is in progress. On the A1 Timebase Control Board, CTR/~W is decoded by PAL IC A1U21 generating address and control signals for both the A1 and A2 assemblies. On the A6 DMA/Gate Board, CTR/~W determines the direction of data flow through DMA Input Buffers (A6U57 and U58) and Interpolator RAM bus buffers (A6U13 and U18).
~CTRD	TTL	A12XA7(41)	A12XA6(125)	CounT hardware ReaD is set low (true) when data is read from the count hardware address space (Event 1 and 2 Counter, Timing Counter, and Interpolator RAMs). ~CTRD is a buffered version of ~BREAD.
~CTWR	TTL	A12XA7(39)	A12XA1B(7) A12XA6(124)	CounT hardware WRite is set low (true) when data is written to the count hardware address space (Event 1 and 2 Counter, Timing Counter, and Interpolator RAMs).
C_CHANNEL	ECL	A12J9(10)	A12A5E(1)	Not Used
~DAC1	TTL	A12XA1B(34)	No Connection	Not Used
~DAC2	TTL	A12XA1B(18)	A12XA2B(18)	Digital-to-Analog Converter 2 is used as a chip select signal for Channel A input signal Trigger Level Control DAC, A2U20.
~DAC3	TTL	A12XA1B(2)	No Connection	Not Used

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~DAC4	TTL	A12XA1B(33)	A12XA2B(33)	Digital-to-Analog Converter 4 is used as a chip select signal for Channel B input signal Trigger Level Control DAC, A2U30.
~DATAEN	TTL	A12XA6(116)	A12XA5H(33)	DATA ENable signal is derived from PAL IC A6U36 and enables the System Buffers located on the A5 ZDT/Count Board. These buffers (A5U43 and U47) buffer data to and from the Count Hardware Data Bus (CTD0-CTD15) and the A5 assembly's data bus (DI/O00-DI/O15).
~DAV	TTL	A12XA8(68)	A12J5(6)	DAta Valid is an HP-IB control line that is used in the "Handshake" sequence. When true (low), indicates that data on the DIO lines is stable and available to be accepted by the receiving device.
DC_OFFSET_A	<1 mV rms	A12XA2A(49)	A12J6(19)	An error voltage that establishes the fine DC relationship between the input and output of the Channel A DC Offset Hybrid, A2U2. When this error voltage is properly adjusted, the hybrid's high frequency response will equal its low frequency over a wide temperature range. DC_OFFSET_A is used for in-factory test purposes only.
DC_OFFSET_B	<1 mV rms	A12XA2A(23)	A12J6(39)	An error voltage that establishes the fine DC relationship between the input and output of the Channel B DC Offset Hybrid, A2U14. When this error voltage is properly adjusted, the hybrid's high frequency response will equal its low frequency over a wide temperature range. DC_OFFSET_B is used for in-factory test purposes only.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~DIO1	TTL	A12XA8(136)	A12J5(1)	DIO1-DIO8 (Data Input/Output) is an 8-bit, bidirectional HP-IB data bus that transmits data across the 5371A's HP-IB interface.
~DIO2	TTL	A12XA8(137)	A12J5(2)	
~DIO3	TTL	A12XA8(138)	A12J5(3)	
~DIO4	TTL	A12XA8(139)	A12J5(4)	
~DIO5	TTL	A12XA8(135)	A12J5(13)	
~DIO6	TTL	A12XA8(134)	A12J5(14)	
~DIO7	TTL	A12XA8(133)	A12J5(15)	
~DIO8	TTL	A12XA8(132)	A12J5(16)	
~DTACK	TTL	A12XA8(35)	A12XA7(35)	Data Transfer ACKnowledge is the DTACK signal for the System Bus. When set low, ~DTACK informs the uP that data sent during a write cycle has been received, or when data placed on the bus is valid during a read cycle is valid. If the 68000 μP does not receive a ~DTACK signal within ~60 μs of read or write, a bus error occurs. ~DTACK signals for the System Bus are generated on the A8 I/O Controller.
ECL10MHZ	ECL	A12XA6(104)	A12XA5A(46)	ECL10MHZ is an input to the A5 ZDT/Count Board's Sequencer IC, A5U29. This signal is derived from the A14 Timebase Multiplier Board's 10 MHz output, buffered by the A1 Timebase Control Board, and then routed to the A6 DMA/Gate Board where it is used as the System Timer Controller's (A6U41) timebase reference. CLK10 is also gated and translated into the ECL10MHZ signal. NOTE: ECL10MHZ is not currently used by the Sequencer IC.
~EOI	TTL	A12XA8(69)	A12J5(5)	End Or Identify is an HP-IB control line used to indicate the end of a multiple-byte message on the HP-IB data bus.
EXTREF	TTL	A12J10(2)	A12XA1F(1)	This 1, 2, 5 or 10 MHz rear-panel input is used as a reference timebase when present. The internal A15 Oven Oscillator 10 MHz reference timebase is used when there

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				is no rear-panel EXTERNAL INPUT present.
EXTSTATE	TTL	A12XA6(8)	A12J6(25)	EXTernal arm input STATE reflects the high or low state of the front-panel EXTERNAL ARM input signal. The 68000 µP reads this status bit via Interrupt PAL (A6U22) located on the A6 DMA/Gate Board. EXTSTATE is also used for in-factory test purposes.
EXT_IN	ECL	A12XA6(15)	A12XA5A(7)	The buffered and conditioned version of the front-panel EXTERNAL ARM input signal. The EXTERNAL ARM has a frequency bandwidth of 100 MHz and can be used to arm many 5371A measurements.
FAN LINE VOTAGE 1	120 VAC ±10%	A16 Power VAC Module (Pin D)	A12J4(2)	This line provides line voltage from A16 Power Module Cable Assembly to the "Fan Control" circuit located on the A12 Motherboard.
FAN LINE VOLTAGE 2	120 VAC ±10%	A12J4(4)	Fan B1 (Pin 1) via cable W8	This linep rovides line voltage from load side of "Fan Control" circuit to Cooling Fan B1 via cable W8.
FAN RETURN PATH 1	120 VAC NEUTRAL	Fan B1 (Pin 2)	A12J4(4) via cable W8	Part of Cooling Fan B1 ac return path from A12 Motherboard to A16 Power Module Cable Assembly.
FAN RETURN PATH 2	120 VAC NEUTRAL	A12J4(1)	A16 Power Module (Pin N)	Part of ac return path from fan B1 to A12 Motherboard via cable W8.
GATE_1	TTL	A12XA4B(32)	Routes to buffer A12U5C(8), then from A12U5C(9) to A12J10(3).	The falling edge of GATE_1 occurs when measurement samples are made. This signal is a buffered version of the IT1 signal. This signal is available at the instrument's rear panel and informs the user when the 5371A is making a measurement.
GATE_2	TTL	A12XA4B(64)	Routes to buffer A12U5B(5), then from A12U5B(6) to A12J10(4).	The falling edge of GATE_2 occurs when measurement samples are made. This signal is a buffered version of the IT2 signal. This signal is available at the instrument's rear panel and informs the user when the

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				5371A is making a measurement.
~HALT	TTL	A12XA7(18)	No Connection	~HALT is used by the A7 Processor Board only during instrument power-up. ~PURST, generated by the A10 Triple Regulator Board, ensures that ~RESET, ~RESETB, and ~HALT are held low at power-up.
HOT	TTL	A12XA9(16)	A12U7C(10)	HOT monitors the internal temperature of the 5371A in case the the Cooling Fan B1 fails or air flow is blocked in some manner. A thermistor, mounted on A9 Double Regulator Board transistor A9Q5, sets HOT high when the internal temperature is too high. The HOT line is latched by the A12 Motherboard "Regulator Control" circuit, which turns off both A9 and A10 power supply assemblies. Both assemblies remain off until either the front-panel STBY-ON power switch is cycled ON-to-STBY-to-ON, or or the ac power cord is disconnected and then reconnected.
HSYNC	TTL	A12XA8(109)	A12J1(5)	Horizontal SYNChronization signal controls the CRT Display raster (beam) horizontal retrace.
ID0A	TTL	A12J7(2)	A12XA1A(13)	IDOA-ID2A, a 3-bit I-Dentification code hard-wired into the input pod installed, informs the 68000 μP which of three input pods are installed in 5371A CHANNEL A pod slot. The three pods that can be used are the HP 54001A, 54002A, or the 54003A.
ID1A	TTL	A12J7(4)	A12XA1A(14)	
ID2A	TTL	A12J7(5)	A12XA1A(40)	

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
ID0B	TTL	A12J8(2)	A12XA1A(16)	ID0B-ID2B, a 3-bit I-Dentification code hard-wired into the input pod installed, informs the 68000 μP which of three input pods are installed in the 5371A CHANNEL B input pod slot. The three pods that can be used are the HP 540001A, 54002A, or 54003A.
ID1B	TTL	A12J8(4)	A12XA1A(17)	
ID2B	TTL	A12J8(5)	A12XA1A(43)	
~IFC	TTL	A12XA8(65)	A12J5(9)	InterFace Clear HP-IB control line is sent by an external system controller to untalk and unlisten the 5371A and initialize the HP-IB to an idle state (no activity on the bus).
~INT1	TTL	A12XA6(138)	A12XA7(66)	The 68000 μP INTerrupt (level 1) is generated at the completion of each individual measurement or block of measurements. ~INT1 is also generated when the ZDT counter registers overflow.
~INT2	TTL	A12XA1B(31)	A12XA7(136)	The 68000 μP INTerrupt (level 2) is set low whenever the oscillator reference frequency source changes from the internal A15 Oven Oscillator to an external 1, 2, 5, or 10 MHz reference frequency applied to the instrument's rear-panel EXTERNAL INPUT connector, or vice versa. ~INT2 is also set low when the A14 Timebase Multiplier Board's phase-locked loop is circuit is out of lock.
~INT3	TTL	A12XA1B(15)	A12XA7(65)	The 68000 μP INTerrupt (level 3) is set low when either an input signal over-voltage condition is detected, an input pod was removed and its absence detected at instrument power-up, or when the A1 Multiplier Board's phase-locked loop is out-of-lock.
~INT4	TTL	A12XA8(86)	A12XA7(86)	The 68000 μP INTerrupt (level 4) is set low after completion of a programmed set of HP-IB or DMA data transfers. The HP-IB Controller IC, A8U50, and the DMA Controller IC,

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				A8U30, are both capable of producing level 4 interrupts.
~INT5	TTL	A12XA8(17)	A12XA7(17)	The 68000 μP INTerrupt (level 5) is set low after detection of a front-panel input by the Keyboard Controller IC, A8U1.
~INT7 (~POWERFAIL)	TTL	A12U10A(3)	A12XA7(44)	The 68000 μP INTerrupt (level 7 is set low whenever the "Power-Fail Detection Control" circuit located on the A12 Motherboard detects a low-voltage condition. This signal informs 68000 μP that it has at least 5 ms before the 5371A will lose power. Within 5 ms, the 68000 μP must suspend operations, open the front-end relays, and perform a checksum on the data stored in back-up CMOS RAMs A7U50 and U51. Once the checksum is complete, the stored data should be protected. The ~POWERFAIL interrupt is the highest level interrupt so it will always get immediate 68000 microprocessor attention.
INTSP1	TTL	No Connection	A12XA6(107)	Not Used
INTSP2	TTL	A12XA4B(34)	A12XA6(38)	INTSP2-INTSP4 is the 4-bit binary equivalent of the resolved time difference between the last gated event-edge trigger, IT2, and the 500 MHz reference clock, CLKA. This 4-bit code is derived by Interpolator 2 (Stop) circuit located on the A4 Interpolator Board.
INTSP3	TTL	A12XA4B(1)	A12XA6(108)	
INTSP4	TTL	A12XA4B(17)	A12XA6(39)	
INTST1	TTL	No Connection	A12XA6(28)	Not Used
INTST2	TTL	A12XA4A(48)	A12XA6(98)	INTST2-INTST5 is the 4-bit binary equivalent of the resolved time difference between the first gated event-edge trigger, IT1, and the 500 MHz reference clock, CLKA. This 4-bit code is derived by Interpolator 1 (Start) circuit located on the A4 Interpolator Board.
INTST3	TTL	A12XA4A(47)	A12XA6(26)	
INTST4	TTL	A12XA4A(46)	A12XA6(96)	
INTST5	TTL	A12XA4A(45)	A12XA6(25)	
IT1	ECL	A12XA5I(1)	A12XA4C(1)	

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				Event-edge Interpolator Trigger signal sent from Sequencer A5U29 to the A4 Interpolator Board's Interpolator 1 (Start) circuit after all prescribed measurement arming conditions have been met. This circuit time resolves IT1 with CLKA to a resolution of 200 ps.
IT2	ECL	A12XA5L(1)	A12XA4F(1)	Event-edge Interpolator Trigger signal sent from Sequencer A5U29 to the A4 Interpolator Board's Interpolator 2 (Stop) circuit after all prescribed measurement arming conditions have been met. This circuit time resolves IT2 with CLKA to a resolution of 200 ps.
~LEDA	TTL	A12XA2A(14)	A12XA8(101)	When ~LEDA is driven low, front-panel CHANNEL A LED (A11DS8) illuminates. When flashing, A11DS8 gives a visual indication that an input signal is triggering the A2 Input Amplifier Board circuitry. ~LEDA exits the A2 assembly, passes through the A12 and A8 assemblies respectively, and then to the A11 Front Panel Board via ribbon cable W5.
~LEDB	TTL	A12XA2A(16)	A12XA8(102)	When ~LEDB is driven low, front-panel CHANNEL B LED (A11DS7) illuminates. When flashing, A11DS7 gives a visual indication that an input signal is triggering the A2 Input Amplifier Board circuitry. ~LEDB exits the A2 assembly, passes through the A12 and A8 assemblies respectively, and then to the A11 Front Panel Board via ribbon cable W5.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
LP	+5.6V dc	A12 Motherboard "Power-Fail Detect" (Junction of resistor A12R2, R3, R24, and anode of diode A12CR16.	A12XA7(115)	LP conserves back-up battery A7BT1 during Standby operation by supplying power to the back-up RAMs A7U50 and A7U51 via the VNV supply. A7CR2 regulates the
~MEDMA	TTL	A12XA8(42)	A12XA7(42)	Memory DMA line is valid (low) only during a DMA cycle. This line is asserted low when the data being being downloaded to the HP-IB is stored in A7 assembly's System Ram. ~MEDMA controls the direction of flow through the A7 assembly's "Global Bus Buffers". When ~MEDMA and ~BGACK are both set low, the Global Bus address buffers change direction, allowing the addresses generated by the DMA Controller IC (A8U30) to gain access to System RAM via the Private Address Bus.
MISC_CLK	TTL	A12XA1A(20)	A12XA2A(20)	MISCellaneous CLocK provides clock that latches control data bits from Count Hardware Data lines CTD0-CTD7. These control bits program Channel A and B input signal conditioning (i.e., termination bias, ± trigger slope, and trigger LED enable).
~NDAC	TTL	A12XA8(66)	A12J5(8)	Not Data ACcepted HP-IB control line is used in the "Handshake" sequence. When false (high), indicates that a device is ready to receive data.
~NRFD	TTL	A12XA8(67)	A12J5(7)	Not Ready For Data HP-IB control line is used in the "Handshake" sequence. When false (high), indicates to the transmitting device that data has been accepted by the receiver.
OFF/~ON	OFF=~+25V ~ON=~+12V	A12XA8(47)	To junction of resistors A12R28 and R29, cathodes of diodes A12CR10 and CR17, pin 2 of opto-isolator A12U9.	OFF/~ON connects directly to front-panel STBY-ON power switch and controls such A12 Motherboard circuits as "Fan Control", "Power-fail Interrupt", and "Off Delay".

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
OVEN	+20 to +30V dc, ~+21 V dc Nominal, with ripple and noise < 30 mV RMS.	A12U11(2)	A12XA15(14,29)	OVEN provides power the A15 Oven Oscillator heater as long as the 5371A is connected to ac power.
OVER_VOLT_A	TTL	A12XA1A(19)	A12XA2A(19)	Toggles to logic low in response to an over-voltage condition. This causes relays in A2 Input Amplifier CHANNEL A input path to open, protecting the input circuitry from damage.
OVER_VOLT_B	TTL	A12XA1A(44)	A12XA2A(44)	Toggles to logic low in response to an over-voltage condition. This causes relays in A2 Input Amplifier CHANNEL B input path to open, protecting the input circuitry from damage.
OVER_V_A	0 ± ~2.7V dc	A12XA2A(46)	A12XA1A(46)	Monitors CHANNEL A input signal path for over-voltage conditions.
OVER_V_B	0 ± ~2.7V dc	A12XA2A(21)	A12XA1A(21)	Monitors CHANNEL B input signal path for over-voltage conditions.
~PURST	TTL	A12XA10B(1)	A12XA7(45)	Power-Up ReSeT is set low for 120 ms (nominal value) after the A10 Triple Regulator Board's +5RAW output reaches approximately +4.5 Volts. This negative pulse pulls both ~RESET and ~HALT low, a requirement that must be met at instrument power-up for complete reset of the 68000 μP.
~RAMCS	TTL	A12XA6(45)	A12XA5H(17)	~RAMCS is connected to the chip select pin 20 of all 12 Measurement RAMs located on the A5 ZDT/Count Board. This line is grounded on the A6 DMA/Gate Board.
~RAMOE	TTL	A12XA6(21)	A12XA5A(26)	When set low, RAM Output Enable line permits reading and writing measurement data to/from A5 ZDT/Count Board's Event and Timing Counter Measurement RAMs, and A6

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
				DMA/Gate Board's Start and Stop Interpolator RAMs.
RAMTC	TTL	A12XA6(9)	A12J6(27)	RAM Terminal Count is the BFUL_W signal delayed by one clock pulse. The delay ensures that 68000 μP interrupt ~INT1 is generated after the last set of measurement data is loaded into memory. RAMTC is also routed used for in-factory test purposes.
REFOUT (10 MHz)	1 V(p-p), Nominal, ac coupled square wave into 50 Ohms. >2 V(p-p), NOMINAL, ac coupled square wave into high impedance. Both limits apply to measurements made at 5371A rear panel.	A12XA1G(1)	A12J10(5)	Buffered 10 MHz rear-panel output derived from A14 Multiplier Board phase-locked loop circuit. From the A14 Multiplier Board, the 10 MHz ECL-level signal is sent to the A1 Timebase Control (via cable W14) for buffering and then routed to the rear-panel 10 MHz OUTPUT. When an external reference is applied to the HP 5371A, this output will match the external reference's stability characteristics but but will always equal 10 MHz.
RELAY_CLK	TTL	A12XA1A(45)	A12XA2A(45)	RELAY CLocK is the clock that latches relay A2K1-K8 control data bits from Count Hardware Data lines CTD0-CTD7 directly to relay driver A2U26.
~REN	TTL	A12XA8(70)	A12J5(17)	Remote ENable HP-IB control line, sent the by the system controller only, enters the 5371A into remote state. This enables the 5371A to respond to interface commands when addressed as a listener.
~RESETB	TTL	A12XA7(135)	A12XA1B(14) A12XA2B(14) A12XA6(136) A12XA8(61) A12U10B(4)	The buffered version of ~RESET. ~RESET line is used on A7 Processor Board exclusively, while ~RESETB is distributed throughout the instrument. The ~RESET line can be pulled low by the A10 Triple Regulator ~PURST line, pressing switch A7S1, or by programming the 68000 μP using the RST instruction.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~SEQCS	TTL	A12XA6(115)	A12XA5H(1)	The SEQuencer Chip Select line is set low while programming the Sequencer's internal registers for the prescribed arming and gating requirements.
SHUTDOWN	TTL	A12U4(3)	A12XA10B(16)	When set high, SHUTDOWN turns off the ±15V supply regulator ICs on the A10 Triple Regulator Board. Since the A9 Double Regulator Board uses voltages generated on the A10 to operate, the A9 shuts down whenever the A10 shuts down. Conditions when SHUTDOWN is set high include switching the front-panel STBY-ON switch to STBY or losing ac power to the instrument.
SINGLE_TTL	TTL	A12XA6(24)	A12XA5A(59)	SINGLE_TTL is decoded from the measurement control word by the A6 DMA/Gate Board and allows the 68000 μP to control single-write measurements.
~SRQ	TTL	A12XA8(64)	A12J5(10)	Service ReQuest HP-IB control line is set low (true) by the 5371A when it requires service by the system controller. The Event Status Enable and Hardware Status Enable register settings define the conditions under which the SRQ message is transmitted. The 5371A does not accept SRQ messages.
SYSIN	ECL	A12XA6(22)	A12XA5A(58)	SYStem INitialization is decoded from the measurement control word by the A6 DMA/Gate Board and provides a reset pulse to the A5 ZDT/Count Board's "RAM Write" circuit before the start of each measurement or block of measurements.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
TG1 TG2	ECL ECL	A12XA6(111) A12XA6(46)	A12XA5H(50) A12XA5H(49)	Gate timing signals TG1 and TG2 are generated by the System Timing IC (A6U41) and are used by the Sequencer IC (A5U29) as the start and stop arming signals when making continuous measurements during INTERVAL Arming mode. The output and pulse width of TG1 and TG2 are each independently controlled by the 68000 μP.
~TRGLGT	TTL	A12XA6(85)	A12XA8(32)	When ~TRGLGT is driven low, front-panel EXTERNAL ARM LED, A11DS9, illuminates. When flashing, A11DS9 gives a visual indication that the EXTERNAL ARM input is triggering the A6 DMA/Gate circuitry. ~TRGLGT exits the the A6 assembly, passes through the A12 and A8 assemblies respectively, and then through cable W5 to the A11 Front Panel Board.
TTR	ECL	A12XA5A(47)	A12XA6(35)	After all measurement arming conditions have been met, Sequencer IC (A5U29) sends Timing TRigger TTR to the System Timing Controller IC (A6U41) instructing it to begin output of gate signals TG1 and TG2.
~UPWR	TTL	A12XA6(34)	A12XA5A(63)	UP WRite is decoded by A6 DMA/Gate Board PAL A6U16 and allows the 68000 μP to control when the Event and Timing ZDT Counters latch their contents into their respective Measurement RAM ICs. ~UPWR is used during diagnostic testing to write measurement data into memory.
VIDEO	Raster (Beam) ON = 0 Raster (Beam) Half-brightness = +2.4V Raster (Beam) Full-brightness = +2.6V	A12XA8(39)	A12J1(3)	Composite signal containing all data that is displayed on the front-panel CRT Display.

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
~VPA	TTL	A12XA7(7)	A12XA8(7)	When set low, the Valid Peripheral Address line informs the 68000 μP that the address currently on the bus decodes to that of a MC6800 family device. The 68000 will respond by executing a synchronous bus cycle. The 68000 μP responds by returning ~BVMA.
~VSYNC	TTL	A12XA8(41)	A12J1(2)	Vertical SYNChronization signal controls the CRT Display raster (beam) vertical retrace.
VT500	+1V dc to +9V dc (PLL Locked)	A12XA1A(22)	A12J6(40)	500 MHz VCO Tuning Voltage is between +1V dc and +9V dc (nominal) when the phase-locked loop circuit, which generates the two 500 MHz reference frequencies, is locked.
~ZDT1ACS	TTL	A12XA6(31)	A12XA5A(29)	Chip select control line for ZDT counter ZDT1A (A5U22) of Event Counter 1 ZDT Chain.
~ZDT1BCS	TTL	A12XA6(14)	A12XA5A(39)	Chip select control line for ZDT counter ZDT1A (A5U15) of Event Counter 1 ZDT Chain.
~ZDT2ACS	TTL	A12XA6(41)	A12XA5H(51)	Chip select control line for ZDT counter ZDT2A (A5U30) of Event Counter 2 ZDT Chain.
~ZDT2BCS	TTL	A12XA6(42)	A12XA5H(54)	Chip select control line for ZDT counter ZDT2B (A5U40) of Event Counter 2 ZDT Chain.
~ZDT3ACS	TTL	A12XA6(105)	A12XA5A(31)	Chip select control line for ZDT counter ZDT3A (A5U28) of Timing Counter ZDT Chain.
~ZDT3BCS	TTL	A12XA6(33)	A12XA5A(30)	Chip select control line for ZDT counter ZDT3B (A5U27) of Timing Counter ZDT Chain.
ZDTA0	TTL	A12XA6(17)	A12XA5A(24)	ZDTA0-ZDTA2 lines allow the addressing of the ZDT's internal registers for programming purposes.
ZDTA1	TTL	A12XA6(89)	A12XA5A(41)	
ZDTA2	TTL	A12XA6(87)	A12XA5A(40)	

Table 7P-1. 5371A Signals (Continued)

MNEMONIC	LOGIC LEVEL/ VOLTAGE RANGE	SOURCE	DESTINATION	FUNCTION
ZDT_ADDRESS	ECL	A12XA5A(64)	A12XA6(106)	Allows alternate reading of Latch 1 (L11 and L21) and Latch 2 (L12 and L22) measurement and interpolator data from count hardware memory without 68000 µP intervention. This is accomplished by toggling bit 0 of the three ZDT Address bits (ZDTA0-ZDTA2).

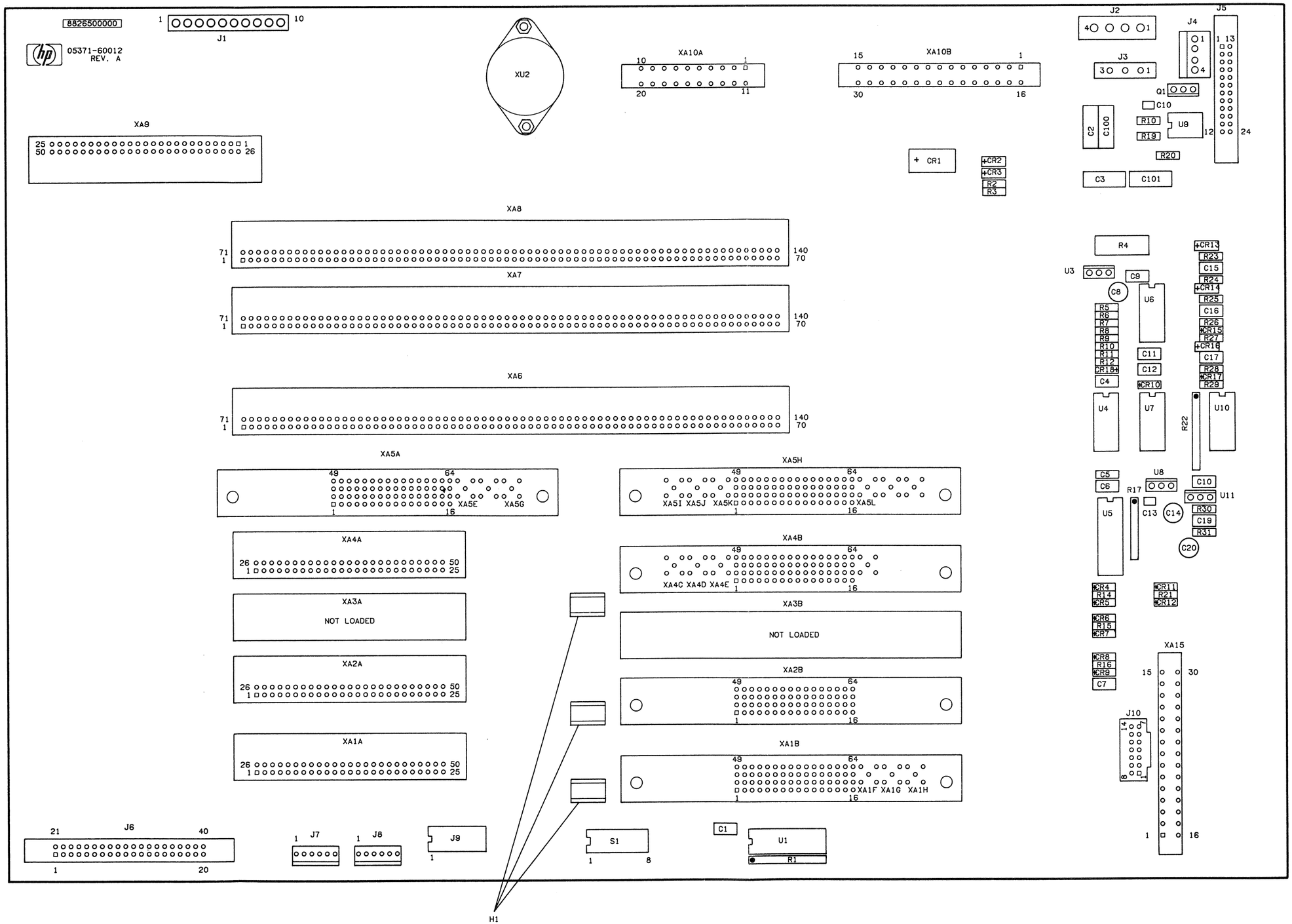

Figure 7P-1. A12 Motherboard Configuration

APP A ARMING

APPENDIX A
ARMING

Table A-1. Continuous Count Measurements

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TI	AUTO	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 or TG2 TC/P1 or TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	EDGE HOLDOFF	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	TIME HOLDOFF	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TI	EVENT HOL-DOFF	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	INTVL SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	EDGE/INTVL	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TI	EDGE HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	TIME HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	EVENT HOL-DOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
CONT. TI	AUTO		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
CONT. TI	EDGE HOLDOFF		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
CONT. TI	TIME HOLDOFF		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
CONT. TI	EVENT HOL-DOFF		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
CONT. TI	INTVL SAMPLE		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
CONT. TI	EDGE/INTVL		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	AUTO	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
FREQ/ PERIOD	INTVL SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	CYCLE SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EDGE SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EDGE/INTVL	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
FREQ/ PERIOD	EDGE/EDGE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EXT GATED,1 CHAN		SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EDGE/ CYCLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
FREQ/ PERIOD	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EDGE SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
FREQ/ PERIOD	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	INTVL SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TOTALIZE	EDGE SAMPLE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	EDGE/INTVL	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	EDGE/EDGE	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	EXT GATED	1 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
TOTALIZE	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	EDGE SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
TOTALIZE	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	PARITY SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/ PARITY	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	EDGE HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	PARITY SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	EDGE/ PARITY	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	PARITY SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/ PARITY	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	EDGE HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	PARITY SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	EDGE/ PARITY	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	AUTO	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE HOLDOFF	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	INTVL SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

Table A-1. Continuous Count Measurements (Continued)

FUNCTION	ARMING MODE	CHANNELS USED	DESCRIPTION
±TI	PARITY SAMPLE	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/INTVL	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE
±TI	EDGE/ PARITY	2 CHAN	SINGLE/DOUBLE/QUADRUPLE WRITE LATCH 1 (L11=L21) OR LATCH 2 (L12=L22) INTERPOLATOR 1, 2, OR 1 & 2 CHA SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN CHB SIGNAL ROUTED TO ZDT1AB OR ZDT2AB CHAIN TG1 OR TG2 TC/P1 OR TC/P2 AUXILIARY SIGNALS: 500 MHz REFERENCE FREQUENCY EVENT HOLDOFF TIME HOLDOFF CYCLE SAMPLE TIME SAMPLE

APPENDIX B
DEFAULT MEASUREMENT SETUPS

B-1. DEFAULT MEASUREMENT SETUP

The Default Measurement Setup (DMS) function allows the 5371A to set up a configuration most likely to give valid measurement result for the currently selected measurement function. When the DMS function is selected (using the DMS command or the front-panel SHIFT, PRESET keys), a number of values are preset to predetermined default conditions. These conditions include source channel, sample size, arming (and the associated arming parameters), and input channel specifications (trigger modes, levels). Math modifiers are disabled, Statistics mode is enabled, and the Numeric "Results + Statistics" screen is displayed. With a single keypress, the measurement is set up and valid measurement results plus statistical analysis results can be obtained.

B-2. General Conditions

When entering the Default Measurement Setup mode, the following general conditions are true for all types of measurements:

- Previous setup is saved in Register 0.
- Math Modifiers are disabled.
- Statistics are enabled.
- Limit Testing is disabled.
- Reference values are set to 0.
- Channel A Trigger mode is set to Repetitive Auto trigger.
- Channel B Trigger mode is set to Repetitive Auto trigger.
- Channel A Attenuation is set to X1.
- Channel B Attenuation is set to X1.
- NUMERIC Display is chosen, showing "Results + Statistics".
- Measurement Sample size is set 50 (measurements per block) except Peak Amplitude measurements where Measurement Sample Size is set to 1.
- Block size is set to 1 (number of measurement blocks).

B-3. Default Setup Values

The default setup values for each measurement type are as follows:

B-4. TIME INTERVAL

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set 50% (positive slope)
Input Mode set to Separate.

B-5. +/-TIME INTERVAL

Arming set to Automatic.
Source Channel set to A→B.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-6. CONTINUOUS TIME INTERVAL

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-7. FREQUENCY

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-8. PERIOD

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-9. TOTALIZE

Arming set to Interval Sampling.
Interval Time set to 10.0 μs.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-10. POSITIVE PULSE WIDTH

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Common.

B-11. NEGATIVE PULSE WIDTH

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope) .
Input Mode set to Common.

B-12. RISETIME

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 20% (positive slope).
Channel B Trigger Level set to 80% (positive slope).
Input Mode set to Common.

B-13. FALLTIME

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 80% (negative slope).
Channel B Trigger Level set to 20% (negative slope).
Input Mode set to Common.

B-14. DUTY CYCLE

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (negative slope).
Input Mode set to Common.

B-15. PHASE

Arming set to Automatic.
Start On Positive Edge of Channel A.
Source Channel set to A relative B (A rel B).
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

B-16. PEAK AMPLITUDE

Arming set to Automatic.
Source Channel set to A.
Channel A Trigger Level set to 50% (positive slope).
Channel B Trigger Level set to 50% (positive slope).
Input Mode set to Separate.

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